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Wirebond Looping Optimization on Critical Stacked-Dies Semiconductor Device

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***Keywords*—** *Wirebond; stacked dies; semicondcuctor; substrate; wirebond loop.*

I. Background of the Study

Assembly manufacturing challenges are inevitable during package development of an advanced substrate-based semiconductor package represented in Fig. 1. One great challenge is the difficulty on wire looping during wirebond process on Die 1 or the bottommost die. A critical aspect to consider is the avoidance of the wire-to-die shorting between the wires and Die 1 especially during the die attach process of Die 2. Hence, looping characterization is critically needed to meet the requirements in wirebonding process.

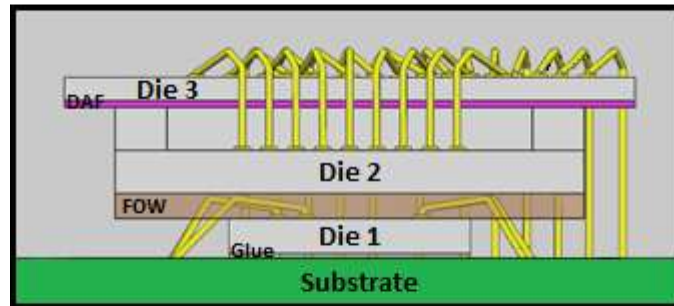

Fig. 1. Package cross-sectional view.

II. Problem Identification

During wirebonding process at Die 1, a criticality in the loop was seen and anticipated due to the succeeding die attach process of Die 2. The condition for the loop was for the top of wire not to touch or short with either the Die 2 or Die 1, assembled on a critical stacked-dies configuration. Furthermore, it is difficult to distinguish visually due to few micron difference as highlighted in Fig. 2.

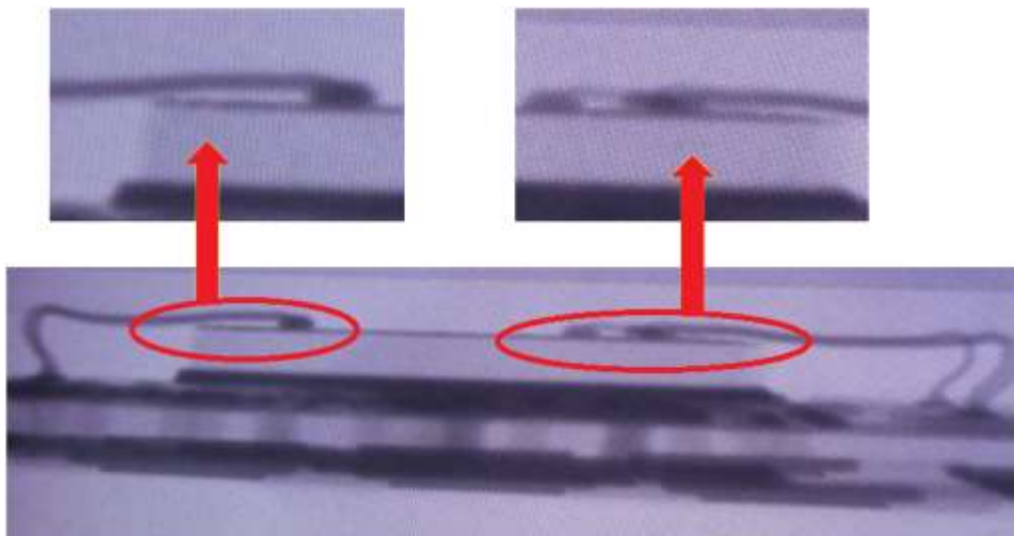
Fig. 2. Tight loop on wirebonding process.

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Optimization of wire looping is very challenging because of the kink. The issue would eventually result to broken wire on neck or nicking as seen on some units in Fig. 3.

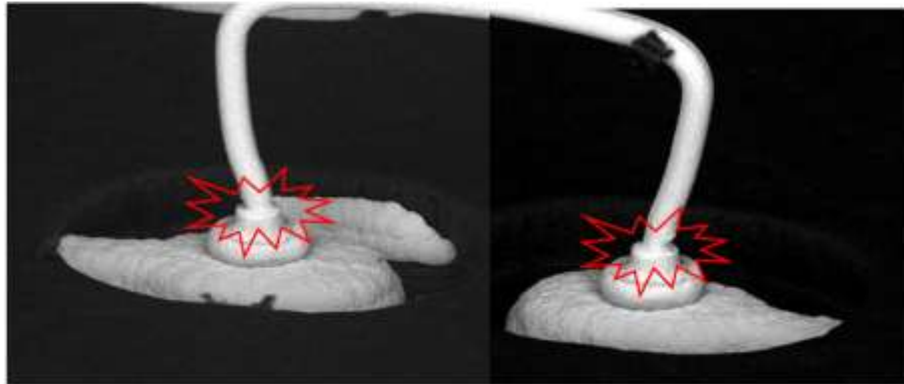

Fig. 3. Nicking occurrence on wirebond.

III. SEMICONDUCTOR PROCESS SOLUTION

An improved solution in wirebonding process is intensively done with wire looping optimization. The solution employs wire looping optimization on the wirebonding process at Die 1 as shown in Fig. 4, preventing high loop that could touch the succeeding Die 2. Moreover, no nicking occurrence was observed during the wirebonding process.

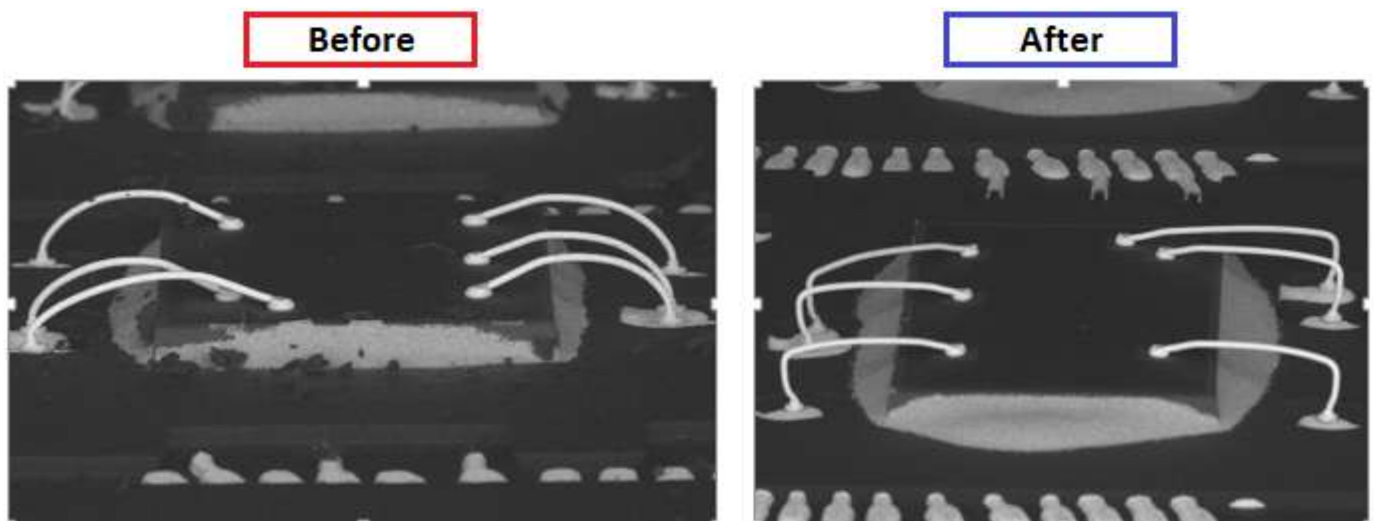

Fig. 4. Improved loop formation with no observed wire nicking defect.

The optimized loop parameter eventually served as the good loop formation, that also passed the destructive wire pull test. The improved loop optimization is considered a key milestone which could be used on any other semiconductor devices with stacked-dies configuration.

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