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A Study of Dynamic Range of Common-Gate with Common-Source Active Balun in CMOS Technology

F.R. Gomez[1,2], J.R. Hizon[1], M.T. De Leon[1]
[1]Microelectronics and Microprocessors Laboratory, University of the Philippines, Diliman, Quezon City, Philippines 1101
[2]New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna, Philippines 4027

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I. Circuit Overview

An active balun (balanced-unbalanced) circuit is a type of transformer that converts signals that are single-ended or unbalanced with respect to ground into signals that are differential or balanced with respect to ground. Fig. 1 illustrates an active balun topology comprising of 2 amplifiers namely common-gate amplifier (M1) and the common-source amplifier (M2). The input signal is applied into the drain node or terminal of transistor M1 and at the same time into the gate node of transistor M2, while the outputs are probed at the drain terminals of M1 and M2. Load resistors R1 and R2 dictate the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

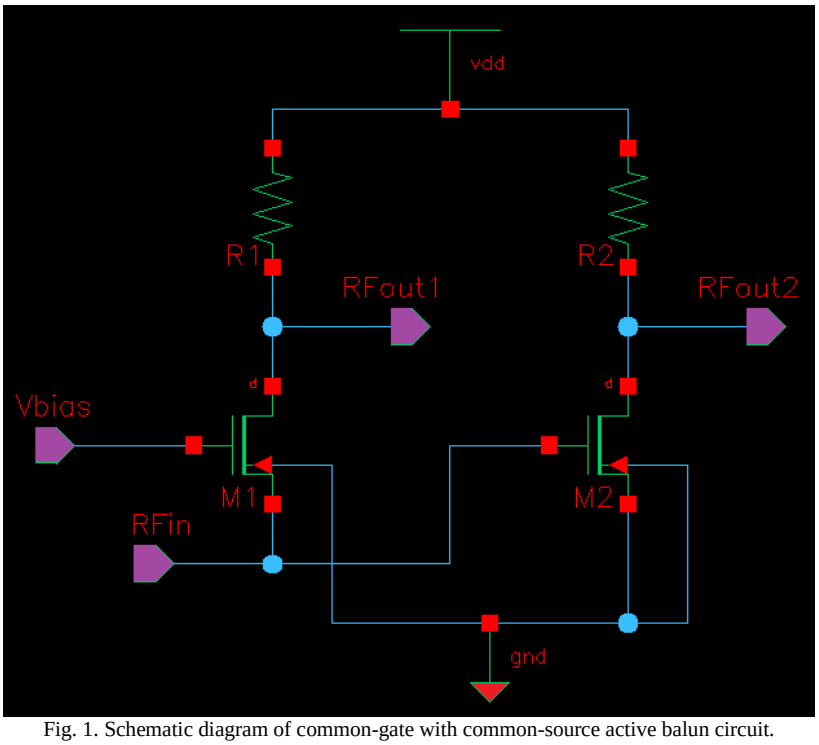

Fig. 1. Schematic diagram of common-gate with common-source active balun circuit.

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. With this, it finds wide applications in analog circuits and its frequency response is of interest. Common-gate topology exhibits no Miller multiplication of capacitances, potentially achieving a wide band [1]. However, the low input impedance may load the preceding stage. Furthermore, since the voltage drop across R1 is typically maximized to obtain the required gain, the DC level of the input signal must be quite low. With the two topologies cascaded to function as an active balun, one major challenge would be to generate balanced gain for the two outputs RFout1 and RFout2 with respect to the input signal RFin, given that the input signal is fed into two different transistor ports.

II. Dynamic Range Analysis

Noise performance is an important design consideration since it determines the vulnerability of the active balun to unwanted signal like the noise. Important design parameters namely dynamic range (DR), signal-to-noise ratio (SNR), and noise figure (NF) can be derived using noise analysis. Dynamic range is the ratio between the maximum signal power that the system can tolerate

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without distortion of the signal to the noise level of the system. Shown in Fig. 2 and 3 are the circuit models with noise sources of common-gate and common-source stages of the active balun, respectively. Note that input resistance Rs is common to both stages. Source capacitance $C_s = C_{sg1} + C_{sb1}$, while drain capacitance $C_d = C_{dg1} + C_{db1} + C1$ for the common-gate stage.

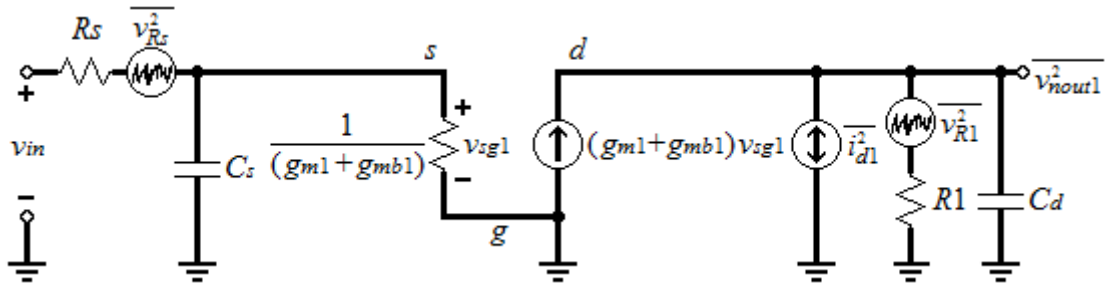

Fig. 2. Common-gate stage model with noise generator.

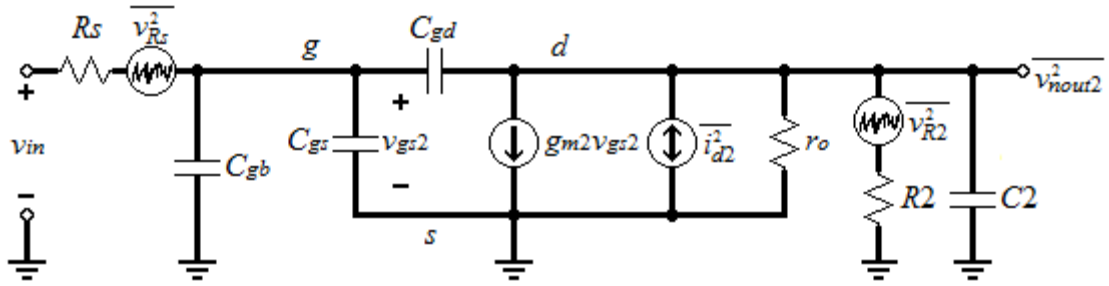

Fig. 3. Common-source stage model with noise generator.

Active balun supplies differential input signal into a differential circuit, hence noise calculation for each of the two output nodes is important. With KCL at node d of Fig. 3, output noise voltage and current of RFout2 are determined in the succeeding equations.

$$\overline{i_{n,out2}^2} = \overline{i_{d,th}^2} + \overline{i_{d,1/f}^2} + \overline{i_{R2}^2} \tag{1}$$

$$\overline{v_{n,out2}^2} = \left[4k_BT\gamma g_{m2}\Delta f + \frac{K_f I_D}{L^2 C_{ox}}\frac{1}{f_{co}}\Delta f + \frac{4k_BT}{R2}\Delta f\right]\left(R2 \| \frac{1}{sC2}\right)^2 \tag{2}$$

At higher frequency, thermal noise of transistor dominates, hence flicker noise could be neglected. Rearranging the expression in (2), output voltage noise of RFout2 could be eventually simplified into (3).

$$\overline{v_{n,out2}^2} = \frac{k_BT}{C2}(1 + \gamma g_{m2} R2) \quad V_{rms}^2 \tag{3}$$

Increasing the resistance R2 increases the overall noise. Output capacitance C2 dictates significantly, if compared to C_{gd}, on the output noise performance. Increasing the capacitance would decrease the output voltage noise but it would also decrease the circuit bandwidth or the cutoff frequency of RFout2. This design tradeoff is inevitable so one should consider the effectiveness of setting or limiting the output capacitance. For the dynamic range computation,

$$DR_2 = 10log\frac{{V_{DD}}^2 \cdot C2}{1 + \gamma g_{m2} R2} + 83.828 \quad dB \tag{4}$$

with C2 given in pF, at room temperature

The output noise voltage and current for RFout1 are determined starting with KCL at node s.

$$\overline{i_{n,out1}^2} = \overline{i_{d1,th}^2} + \overline{i_{d1,1/f}^2} + \overline{i_{R1}^2} \tag{5}$$

$$\overline{v_{n,out1}^2} = \left[4k_BT\gamma(g_{m1} + g_{mb1})\Delta f + \frac{K_f I_{D1}}{L^2 C_{ox}}\frac{1}{f_{co}}\Delta f + \frac{4k_BT}{R1}\Delta f\right]\left(R1 \| \frac{1}{sC_d}\right)^2 \tag{6}$$

With effect of flicker noise neglected at higher frequency,

$$\overline{v_{n,out1}^2} = \frac{k_BT}{C_{dg1} + C_{db1} + C1} \cdot [1 + \gamma(g_{m1} + g_{mb1})R1] \quad V_{rms}^2 \tag{7}$$

If output capacitance C1 dominates the other capacitance C_{dg1} and C_{db1}, expression in (7) could be simplified as

$$\overline{v_{n,out1}^2} = \frac{k_BT}{C1}[1 + \gamma(g_{m1} + g_{mb1})R1] \quad V_{rms}^2 \tag{8}$$

Increasing the resistance R1 increases the overall noise while increasing the load capacitance C1 decreases the circuit noise. But increasing the capacitance C1 would also decrease the circuit bandwidth or the cutoff frequency of RFout1. This design tradeoff is inevitable so one should consider the amount of output capacitance.

Owing to the low input impedance of the common-gate stage circuit, and thus the common-gate with common-source active balun, the input-referred noise current is not negligible even at low frequencies [1]. To calculate the input-referred noise voltage, input of Fig. 2 is shorted to ground and equated to the output noise of the circuit with flicker noise neglected. Input-referred noise voltage is hence computed as

$$\overline{v_{n,in}^2} = 4k_B T \frac{\gamma g_{m1} + \frac{1}{R1}}{(g_{m1} + g_{mb1})^2} \tag{9}$$

An important drawback of common-gate configuration is that it directly refers the noise current generated by the output load to the input. The effect arises because such topology provides no current gain, a point contrast to common-source configuration [1]. The expression of the input noise in (9) will be used for the computation of the noise factors and noise figures for the two outputs. Assuming output load C1 dominates the output capacitance, dynamic range is calculated as

$$DR_1 = 10log\frac{{V_{DD}}^2 \cdot C1}{1 + \gamma(g_{m1} + g_{mb1})R1} + 83.828 \;\; dB \qquad \text{with C1 in pF, at room temperature} \tag{10}$$

The very weak signal received by the radio frequency (RF) circuit makes the input signal very susceptible to noise. The existence of noise is essentially due to the fact that electrical charge is not continuous but rather carried in discrete amounts equal to the electron charge [2]. The study of noise through dynamic range analysis is important because it represents a lower limit to the size of the electrical signal that can be amplified by the RF circuit without significantly deteriorating the signal quality. Hence it is critically important that the common-gate with common-source active balun contributes as little noise as possible in the RF receiver.

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