International Journal of Scientific Engineering and Science
Volume 3, Issue 8, pp. 77-79, 2019. ISSN (Online): 2456-7361

Large-Signal Analysis of a 1V Common-Gate with Common-Source Active Balun Circuit

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Keywords— *Active balun; large-signal analysis; common-gate with common source acitve balun; saturation region.*

I. OVERVIEW

An active balun (balanced-unbalanced) circuit is a type of transformer that converts signals that are single-ended or unbalanced with respect to ground into signals that are differential or balanced with respect to ground. Fig. 1 illustrates an active balun topology comprising of 2 amplifiers namely common-gate amplifier (M1) and the common-source amplifier (M2). The input signal is fed into the drain node or terminal of M1 and into the gate node of M2, while the outputs are probed at the drain terminals of M1 and M2. Load resistors R1 and R2 dictate the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

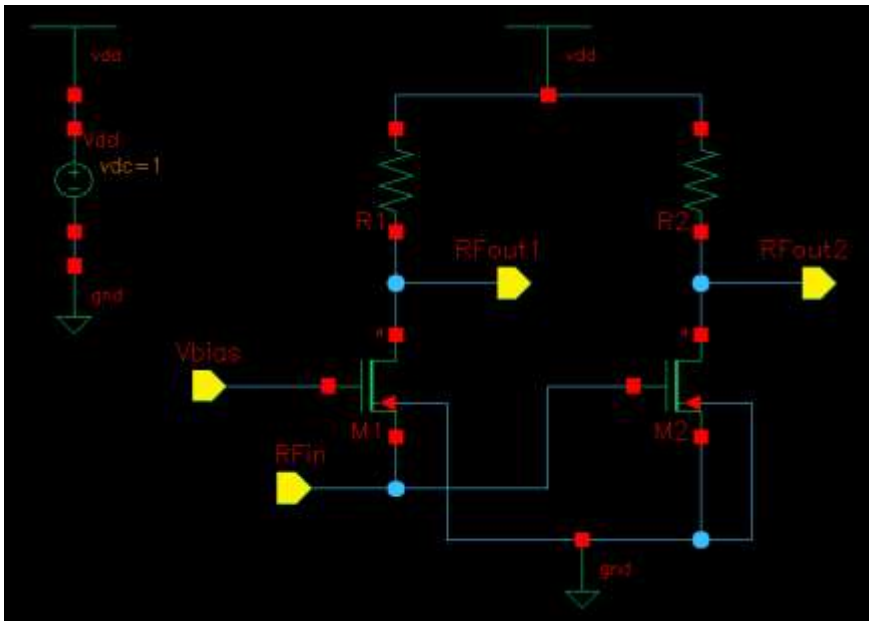

Fig. 1. Common-gate with common-source active balun circuit schematic.

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. With this, it finds wide applications in analog circuits and its frequency response is of interest. Common-gate topology exhibits no Miller multiplication of capacitances, potentially achieving a wide band [1-2]. However, the low input impedance may load the preceding stage. Furthermore, since the voltage drop across R1 is typically maximized to obtain the required gain, the direct current (DC) level of the input signal must be quite low. With the two topologies cascaded to function as an active balun, one major challenge would be to generate balanced gain for the two outputs RFout1 and RFout2 with respect to the input signal RFin, given that the input signal is fed into two different transistor ports.

II. LARGE-SIGNAL ANALYSIS

Direct current (DC) analysis or large-signal analysis is critical in the design of the active balun circuit as it determines the optimum operating point and bias conditions. Moreover, large-signal values are crucial to define the small-signal parameters. On the other hand, small-signal parameters are important to determine the frequency response of the circuit like the maximum frequency of operation and the effective bandwidth, and ensuring that the designed active balun would produce the target gain or attenuation at the desired frequency of operation.

To achieve the maximum output swing for M2, VRFout2 (or simply V2) should be between supply voltage (V_{DD}) and the

Volume 3, Issue 8, pp. 77-79, 2019. ISSN (Online): 2456-7361

saturation voltage (V_{DSAT}) or the overdrive voltage (V_{OV}) of the transistor, ensuring also that the transistor operates at the saturation region. With V_{DD} = 1V, and V_{OV} set to 200mV, the output at RFout2 could swing from 0.2V to 1V. With the said output swing range, output DC voltage (or bias voltage) V2 is therefore computed as

$$V_{DD} > V2 \geq V_{DSAT2} \quad \rightarrow \quad 1V > V2 \geq 0.2V \tag{1}$$

$$V2 = V_{RFout2} = \frac{V_{DD} + V_{OV2}}{2} = \frac{1V + 0.2V}{2} = 0.6V \tag{2}$$

Input bias voltage (VRFin or simply V_{IN}) is the same as the gate voltage (V_{G2}) of M2 and the source voltage (V_{S1}) of M1. To satisfy the condition $V_{DS2} \geq V_{DSAT2} = V_{OV}$, input voltage ($V_{IN}$) should be properly set. With threshold voltage (V_t) set to 400mV,

$$V_{DS2} = V_{GS2} - V_t \geq V_{DSAT2} \quad \rightarrow \quad (V_{IN} - 0) - 0.4V = 0.2V \tag{3}$$

$$V_{IN} = 0.6V \tag{4}$$

With V_{IN} as the source voltage (V_{S1}) of transistor M1, output DC voltage for RFout1 which is V1 (or VRFout1) could be calculated for maximum output swing.

$$V_{DD} > V1 \geq V_{IN} \quad \rightarrow \quad 1V > V1 \geq 0.6V \tag{5}$$

$$V1 = V_{RFout1} = \frac{V_{DD} + V_{IN}}{2} = \frac{1V + 0.6V}{2} = 0.8V \tag{6}$$

Maximum output swing could be achieved at output DC voltage V1 set to 0.8V and at V2 set to 0.6V. To compute for the proper biasing of transistor M2, with input voltage kept at minimum allowed which is at 0.6V,

$$V_{DS1} = V_{GS1} - V_t \geq V_{DSAT1} \quad \rightarrow \quad (V_{BIAS} - V_{IN}) - 0.4V = 0.2V \tag{7}$$

$$V_{BIAS} = 1.2V \tag{8}$$

If overdrive voltage (V_{OV}) is set to 100mV for both transistors M1 and M2, output swings for V1 and V2 could be adjusted. Also, input voltage (V_{IN}) and bias voltage (V_{BIAS}) for M2 could be lowered. Recalculations are shown in the succeeding expressions.

$$V2 = \frac{V_{DD} + V_{OV2}}{2} = \frac{1V + 0.1V}{2} = 0.55V \tag{9}$$

$$V_{IN} = 0.4V + 0.1V = 0.5V \tag{10}$$

$$V1 = \frac{V_{DD} + V_{IN}}{2} = \frac{1V + 0.5V}{2} = 0.75V \tag{11}$$

$$V_{BIAS} = V_{IN} + 0.4V + 0.1V = 1V \tag{12}$$

With input DC voltage (V_{IN}) set to 0.5V, amplifier efficiency in terms of gmoverId could be derived for the two branches or outputs.

$$g_{m1} = \frac{\delta I_{DS1}}{\delta V_{GS1}} = \mu C_{ox} \frac{W_1}{L_1} (V_{GS1} - V_t)(1 + \lambda V_{DS1}) \tag{13}$$

$$g_{m2} = \frac{\delta I_{DS2}}{\delta V_{GS2}} = \mu C_{ox} \frac{W_2}{L_2} (V_{GS2} - V_t)(1 + \lambda V_{DS2}) \tag{14}$$

Substituting the expression for the drain current or drain-to-source current (I_{DS}) into the tansconductance (g_m),

$$g_{m1} = \frac{\delta I_{DS1}}{\delta V_{GS1}} = \frac{2I_{DS1}}{V_{GS1} - V_t} = \frac{2I_{DS1}}{V_{BIAS} - V_{IN} - V_t} \tag{15}$$

$$\frac{g_{m1}}{I_{DS1}} = \frac{2}{V_{BIAS} - V_{IN} - V_t} = gmoverId1 \tag{16}$$

$$g_{m2} = \frac{\delta I_{DS2}}{\delta V_{GS2}} = \frac{2I_{DS2}}{V_{GS2} - V_t} = \frac{2I_{DS2}}{V_{IN} - V_t} \quad (17)$$

$$\frac{g_{m2}}{I_{DS2}} = \frac{2}{V_{IN} - V_t} = gmoverId2 \quad (18)$$

For low power design, higher gmoverId is recommended. To achieve such, V_{IN} and V_{BIAS} should be optimized. With bias voltage (V_{BIAS}) fixed, increasing the input voltage (V_{IN}) increases the efficiency of M1 in terms of gmoverId1. On the other hand, increasing V_{IN} would decrease the efficiency of M2 in terms of gmoverId1. Lowering the drain current or supply current (I_{DS}) would also mean lowering g_m to maintain the efficiency for low power consumption. With this, there is a limit in the efficacy of optimizing the input voltage (V_{IN}), bias voltage (V_{BIAS}) and supply current (I_{DS}) to maximize the efficiency in terms of gmoverId.

As previously assumed, V_{OV} is set to 100mV for minimum attenuation and/or maximum voltage swing in outputs RFout1 and RFout2 with respect to the input RFin.

Transistor dimensions, particularly the transistor gate widths W1 and W2 of M1 and M2, respectively, could be approximated with values inputted in the square-law model in (19) and (20), respectively.

$$I_{DS1} = \frac{\mu C_{ox}}{2}\frac{W1}{L}[(V_{BIAS} - V_{IN}) - V_t]^2[1 + \lambda(V1 - V_{IN})] \quad (19)$$

$$I_{DS2} = \frac{\mu C_{ox}}{2}\frac{W2}{L}(V_{IN} - V_t)^2(1 + \lambda \cdot V2) \quad (20)$$

Drain current (I_{DS}) dictates the transistor gate width (W). Increasing the supply current will require larger transistor width. As mentioned in the earlier section, larger W would result to a larger transistor gate area which in turn increases the parasitic capacitances. Thus design tradeoff for supply current (I_{DS}) and transistor sizing is inevitable.

ACKNOWLEDGMENT

The authors would like to acknowledge the valuable support of the Department of Science and Technology (DOST), DOST-PCASTRD, DOST-ERDT, and the Microelectronics and Microprocessors Laboratory (Microlab) of the University of the Philippines. Author F.R. Gomez is thankful to the STMicroelectronics Calamba New Product Development & Introduction (NPD-I) team and the Management Team for the usual great support.

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