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Analysis on Total Harmonic Distortion of CMOS Common-Gate with Common-Source Active Balun Circuit

Frederick Ray I. Gomez[1,2], John Richard E. Hizon[2]
[1]New Product Development & Introduction Department, STMicroelectronics, Inc., Calamba City, Laguna, Philippines 4027
[2]Microelectronics and Microprocessors Laboratory, University of the Philippines, Diliman, Quezon City, Philippines 1101

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I. Circuit Overview

This active balun is comprised of 2 amplifiers namely common-gate amplifier (with transistor M1) in the 1st stage and common-source amplifier (with transistor M2) in the 2nd stage as shown in the Fig. 1. The input signal is fed into the drain of M1 and into the gate of M2, while the outputs are probed at the drains of M1 and M2. Load resistors R1 and R2 indicate the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

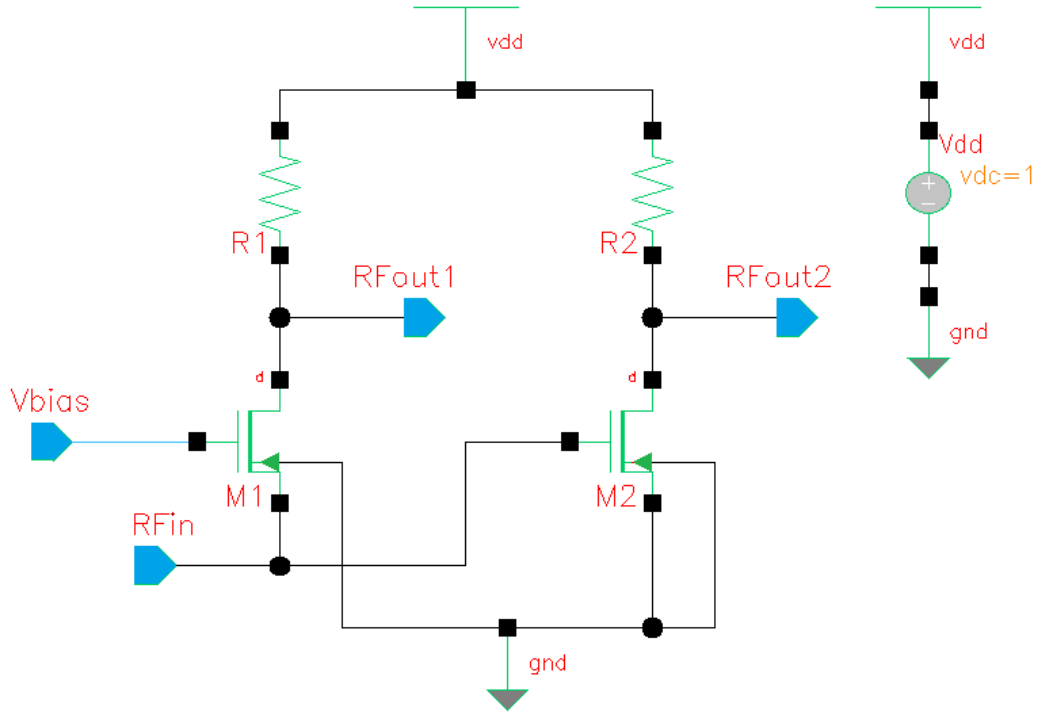

Fig. 1. Common-gate with common-source active balun circuit schematic.

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. With this, it finds wide applications in analog circuits and its frequency response is of interest. Common-gate topology exhibits no Miller multiplication of capacitances, potentially achieving a wide band [1]. However, the low input impedance may load the preceding stage. Furthermore, since the voltage drop across R1 is typically maximized to obtain the required gain, the DC level of the input signal must be quite low. With the two topologies cascaded to function as an active balun, one major challenge would be to generate balanced gain for the two outputs RFout1 and RFout2 with respect to the input signal RFin, given that the input signal is fed into two different transistor ports.

II. Total Harmonic Distortion

A critical parameter that should also be considered in the design of common-gate with common-source active balun implemented in a complementary metal-oxide semiconductor (CMOS) technology is the total harmonic distortion (THD). THD,

which is also a linearity parameter, is the percentage of the inherent harmonics with respect to the fundamental signal. Ideally, THD is zero, but since this is not really the case for transistors and transistor amplifiers, THD should then be minimized.

For a general starting equation, total input voltage (V_{in}) is assumed to be the sum of direct current (DC) input V_{IN} and alternating current (AC) input v_{in}, as a function of time. AC input v_{in} could be further expressed as vrfcosωt, where vrf is the peak value of v_{in}.

$$Vin(t) = V_{DC} + V_{AC} = V_{IN} + v_{in} = V_{IN} + vrf\cos\omega t \tag{1}$$

For RFout1, total drain current (I_{ds}) is expressed as

$$I_{ds1}(t) = \frac{\beta}{2}[V_{GS} - V_t]^2 = \frac{\beta}{2}\{[V_{BIAS} - (V_{IN} + v_{in})] - V_t\}^2 \tag{2}$$

$$I_{ds1}(t) = \frac{\beta}{2}\left[\left({V_{y1}}^2 + \frac{vrf^2}{2}\right) - 2V_{y1}\,vrf\cdot\cos\omega t + \frac{vrf^2}{2}\cdot\cos 2\omega t\right] \tag{3}$$

$$with\ V_{y1} = V_{BIAS} - V_{IN} - V_t\ , v_{in} = vrf\cos\omega t\ , \beta = \mu C_{ox}\frac{W}{L} \tag{4}$$

The drain current has three terms, and substituting back the expression for Vy1, the terms are given as

$$I_{0f1} = \frac{\beta}{2}\left[(V_{BIAS} - V_{IN} - V_t)^2 + \frac{vrf^2}{2}\right] = I_{DC} \rightarrow \text{DC term} \tag{5}$$

$$I_{1f1} = \frac{\beta}{2}[2vrf(V_{IN} + V_t - V_{BIAS})] \rightarrow \text{Amplitude of 1st harmonic} \tag{6}$$

$$I_{2f1} = \frac{\beta}{2}\left(\frac{vrf^2}{2}\right) \rightarrow \text{Amplitude of 2nd harmonic} \tag{7}$$

THD of the RFout1 which is the common-gate stage of the active balun, could now be determined.

$$THD_1 = \frac{vrf}{-4[(V_{BIAS} - V_{IN}) - V_t]} = -\frac{vrf}{4V_{OV}} = -\frac{vrf}{8}\frac{g_{m1}}{I_{DS1}} \tag{8}$$

Minimizing the overdrive voltage (V_{OV}) of transistor M1 would result to higher THD. And increasing the efficiency in terms of gmoverId would also result to higher THD. With this, there is a limit in the effectiveness of optimizing V_{OV} and gmoverId to minimize the total harmonic distortion.

Now for the RFout2, which is that of the common-source stage, total drain current is expressed as

$$I_{ds2}(t) = \frac{\beta}{2}[V_{GS} - V_t]^2 = \frac{\beta}{2}\{[(V_{IN} + v_{in}) - 0] - V_t\}^2 \tag{9}$$

$$I_{ds2}(t) = \frac{\beta}{2}\left[\left({V_{y2}}^2 + \frac{vrf^2}{2}\right) + 2V_{y2}\,vrf\cdot\cos\omega t + \frac{vrf^2}{2}\cdot\cos 2\omega t\right] \tag{10}$$

$$with\ V_{y2} = V_{IN} - V_t\ \ and\ \ v_{in} = vrf\cos\omega t \tag{11}$$

The drain current has three terms, given as

$$I_{0f2} = \frac{\beta}{2}\left[(V_{IN} - V_t)^2 + \frac{vrf^2}{2}\right] = I_{DC} \rightarrow \text{DC term} \tag{12}$$

$$I_{1f2} = \frac{\beta}{2}[2vrf(V_{IN} - V_t)] \rightarrow \text{Amplitude of 1st harmonic} \tag{13}$$

$$I_{2f2} = \frac{\beta}{2}\left(\frac{vrf^2}{2}\right) \rightarrow \text{Amplitude of 2nd harmonic} \tag{14}$$

Total harmonic distortion of the RFout2 which is the common-source stage of the active balun, could now be generated.

$$THD_2 = \frac{vrf}{4(V_{IN} - V_t)} = \frac{vrf}{4(V_{GS2} - V_t)} = \frac{vrf}{4V_{OV}} = \frac{vrf}{8}\frac{g_{m2}}{I_{DS2}} \quad (15)$$

It can be observed that minimizing the overdrive voltage (V_{OV}) of transistor M2 would result to higher THD. Increasing the efficiency in terms of gmoverId would also result to higher THD. With this, there is a limit in the effectiveness of optimizing V_{OV} and the efficiency gmoverId to minimize the distortion.

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