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Process and Design Optimization of Electronic Package with Complex Stacked Dice Configuration

Rennier S. Rodriguez, Frederick Ray I. Gomez
New Product Development & Introduction Department, Back-End Manufacturing & Technology, STMicroelectronics, Inc.
Calamba City, Laguna, Philippines 4027

***Abstract*—** *Package design is one of the key steps prior fabrication and assembly of semiconductor electronic devices. This paper presents the advantage of securing a robust design architecture for specailized electronic devices to minimize the potential show stopper in the realization of high-end technology during assembly manufacturing.*

***Keywords*—** *Stacked dice; electronic device; semiconductor; process improvement; package design.*

I. INTRODUCTION

Miniaturization plays a key role in the future direction of semiconductor electronic packaging due to wide portfolio of applications in various fields of electronic system such as automotive, mobile phones, smart devices, etc., as depicted in Fig. 1. The demand for smaller devices leads to realize that the transition of "moving parts" into nanoscale or microscopic version can make a "watch-size" gadget equipped with different kind of reliable features.

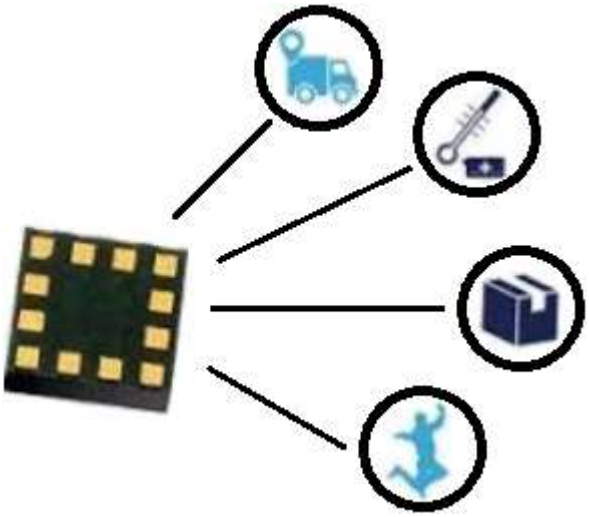

Fig. 1. Examples of applications of a specialized electronic device.

Typically, the external appearance of a specialized semiconductor electronic package (hereinafter referred to as Device A) is something similar to other surface mount devices such as the ball grid array (BGA) and quad flat no-leads (QFN) products. But looking inside its internal composition, the architecture and design of the aforementioned device is different from typical structure of integrated circuit (IC). There are different packaging designs for Device A in semiconductor industry, and usually it is composed of at least two different kinds of silicon die technology configured or assembled in a stacked dice configuration in Fig. 2. In actual application, the two dice are connected into the metal inter-layers of the substrate which later be attached to the electronic boards.

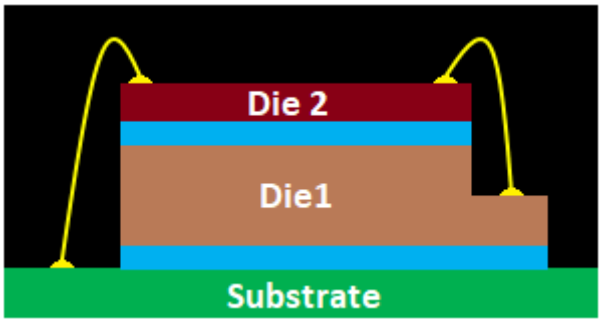

Fig. 2. Stacked dice configuration.

II. PROBLEM IDENTIFICATION

The packaging method for electronic devices particularly Device A is already existing for some semiconductor companies however there are some instances that the known assembly techniques are being challenged in terms of its capability in providing robust ideas in the packaging field.

Design clearance is one of the detractors in the package design of Device A wherein a tighter clearance increases the probability of assembly rejection such as exposed die, exposed wire, or cut wires. Clearance is an important matter in the design stage since this is used to anticipate the machine tolerances and variation during assembly. Due to the consideration to package height and clearance requirement, a package design illustrated in Fig. 3 was proposed.

Fig. 3. Device A package cross-section view.

The Die 1 (bottom die) in between the substrate and Die 2 (top die) is unbalanced with respect to the center position leaving a portion of Die 2 protruding on one side.

During prototype builds, issues specific to worst silicon die tilting is highlighted, as shown in Fig. 4. The occurrence of the

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die tilting is localized to an identified corners of the die where it is constantly located on the protruded part of Die 2.

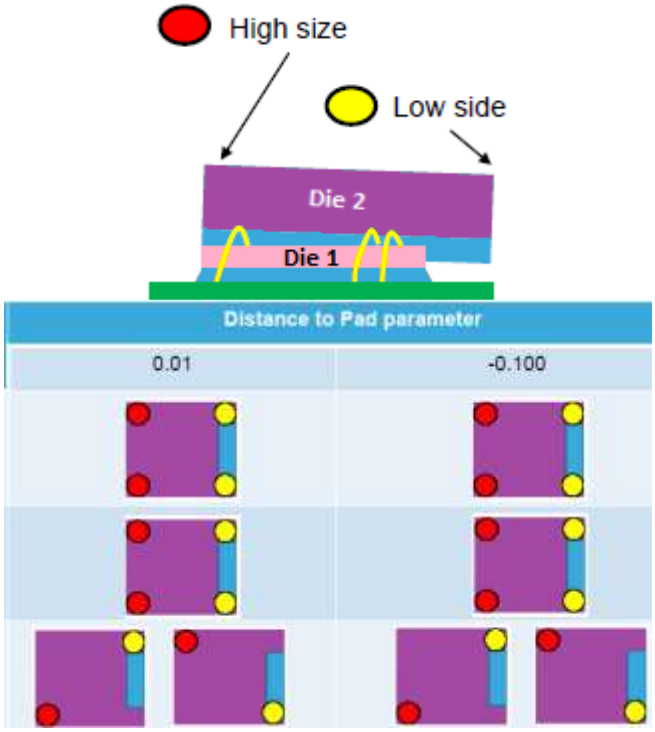

Fig. 4. Localized die tilt.

The tilting behaviour for different die situation is illustrated by red and yellow coloration wherein the yellow circle identifies the lower side and the red circle identifies the higher side. Moreover, the tilting is measured by the difference of the higher side and lower side.

III. Solution, Results and Discussion

Through process and design augmentation and optimization, the current design is modified to a more robust manufacturable architecture. This is supported through fishbone analysis and prototype evaluations of the current vs new design. As shown in Fig. 5, two different designs were processed in parallel, wherein the architecture design with Die 1 at the center position shows positive result in terms of silicon tilting. The "offset" architecture design in this case shows similar result as achieved from the prototype build with localized tilting of silicon die observed.

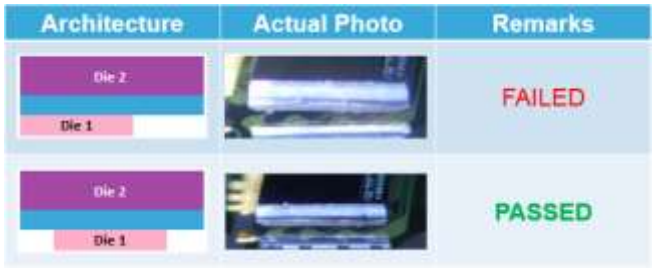

Fig. 5. Summary of evaluation.

Analysis of variance (ANOVA) for die tilt in Fig. 6 shows that the tilt acquired during the evaluation is better on Die 1 with center position as compared to the "offset" architecture.

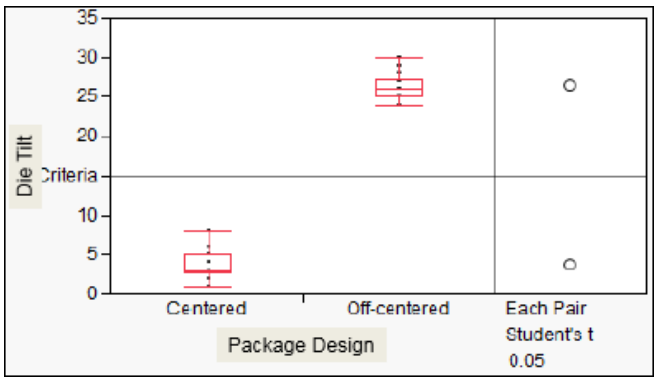

Fig. 6. Statistical comparison.

The behaviour of worst silicon die tilting on "offset" architecture design can be explained by momentum principle. The velocity of the bondhead holding the Die 2 in Fig. 7 during bonding process pushes the die more on the protruded part than the opposite side which has Die 1 to support some weight. The design this time in Fig. 8 shows balanced distribution for Die 2 bonding on both sides with respect to the bottom die or Die 1.

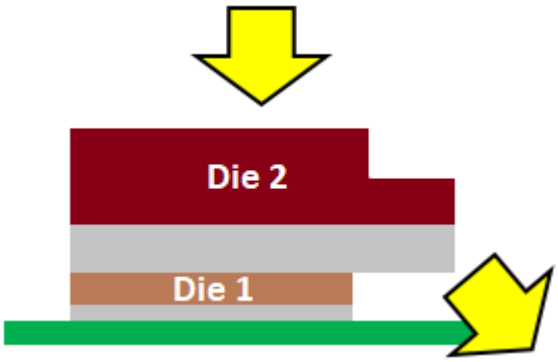

Fig. 7. Moment direction "offset" architecture..

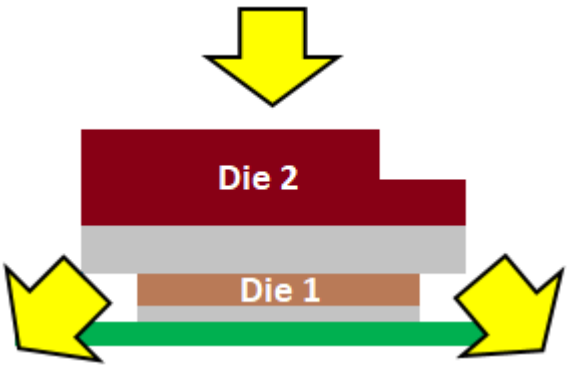

Fig. 8. Moment direction center architecture.

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