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Differential Active Balun Circuit DC Analysis

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I. OVERVIEW

The differential active balun shown in Fig. 1 is composed of 3 transistors namely M1 and M2 for the differential output, and M3 for the tail current. The input signal is applied at the input of one of the differential pair transistors and will ideally split equally between the pair with same amplitude and 180 degrees phase shift. Interestingly, this active balun topology is capable of producing gain.

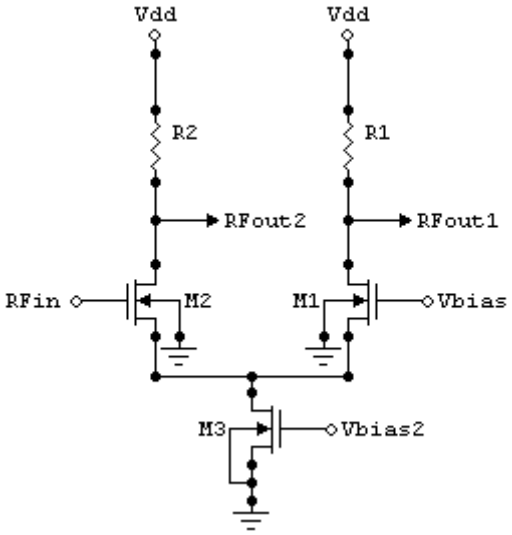

Fig. 1. Differential active balun circuit schematic diagram.

II. DC ANALYSIS

To have a larger headroom for transistors M1 and M2, transistor M3 which acts as the tail current that supplies the M1 and M2 branches should maintain just enough drain-to-source voltage (V_{DS3}). Through the direct current (DC) analysis, setting the drain-to-source voltage (V_{DS}) with V_{DSAT} or V_{OV} for all transistors could maximize the output swing for outputs RFout1 and RFout2. Proper DC input bias should be observed to realize good efficiency in terms of gmoverId. With supply voltage (V_{DD}) set to 1V, overdrive voltage (V_{OV}) set to 200mV, threshold voltage (V_t) set to 400mV, and with the two outputs balanced, input and output DC voltages are computed as

$$V_{DD} > V1 \geq V_{DSAT1} + V_{DSAT3} \quad \rightarrow \quad 1V > V1 \geq 0.4V \tag{1}$$

$$V1 = V_{RFout1} = \frac{V_{DD} + V_{OV1} + V_{OV3}}{2} = \frac{1V + 0.4V}{2} = 0.7V \tag{2}$$

$$V_{DD} > V2 \geq V_{DSAT2} + V_{DSAT3} \quad \rightarrow \quad 1V > V2 \geq 0.4V \tag{3}$$

$$V2 = V_{RFout2} = \frac{V_{DD} + V_{OV2} + V_{OV3}}{2} = \frac{1V + 0.4V}{2} = 0.7V \tag{4}$$

Maximum output swing could be achieved at output DC voltages V1 and V2 both set to 0.7V. With V_{DS3} of tail current branch M3 kept at minimum value for saturation region condition, biasing of M3 is computed as

$$V_{DS3} = V_{GS3} - V_t \geq V_{DSAT3} \quad \rightarrow \quad (V_{BIAS2} - 0) - 0.4V = 0.2V \tag{5}$$

$$V_{BIAS2} = 0.6V \tag{6}$$

To maintain the saturation region condition for both M1 and M2 transistors, input voltage V_{RFin} (or simply V_{IN}) at M2 and bias voltage V_{BIAS} of M1 should be properly set. With threshold voltage V_t set to 400mV, and source voltage V_{S2} of M2 equal to the minimum V_{DS3} of M3 which is at V_{OV},

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$$V_{DS2} = V_{GS2} - V_t \geq V_{DSAT2} \rightarrow (V_{IN} - 0.2V) - 0.4V = 0.2V \quad (7)$$

$$V_{IN} = 0.8V \quad (8)$$

$$V_{DS1} = V_{GS1} - V_t \geq V_{DSAT1} \rightarrow (V_{BIAS} - 0.2V) - 0.4V = 0.2V \quad (9)$$

$$V_{BIAS} = 0.8V \quad (10)$$

If $V_{IN} = V_{BIAS}$, then the gate-source potential for both transistors M1 and M2 is equal, that is $V_{GS1} = V_{GS2}$. However, the impedance of M3 which acts as a current source is not as high as required because of non-ideality caused by parasitics at high frequency. This results in unequal signal distribution, hence affecting the gain balance and phase difference of the circuit. One way to mitigate this imbalance is to adjust the load resistors R1 and R2.

With input bias voltage V_{IN} and voltage bias V_{BIAS2} of M2 derived, circuit efficiency in terms of gmoverId could be computed for the two branches or outputs.

$$g_{m1} = \frac{\delta I_{DS1}}{\delta V_{GS1}} = \mu C_{ox} \frac{W_1}{L_1}(V_{GS1} - V_t)(1 + \lambda V_{DS1}) \quad (11)$$

$$g_{m2} = \frac{\delta I_{DS2}}{\delta V_{GS2}} = \mu C_{ox} \frac{W_2}{L_2}(V_{GS2} - V_t)(1 + \lambda V_{DS2}) \quad (12)$$

Substituting the expression for the drain current (I_{DS}) into the transconductance (g_m),

$$g_{m1} = \frac{\delta I_{DS1}}{\delta V_{GS1}} = \frac{2I_{DS1}}{V_{GS1} - V_t} = \frac{2I_{DS1}}{V_{BIAS} - V_{DS3} - V_t} \quad (13)$$

$$\frac{g_{m1}}{I_{DS1}} = \frac{2}{V_{BIAS} - V_{DS3} - V_t} = gmoverId1 \quad (14)$$

$$g_{m2} = \frac{\delta I_{DS2}}{\delta V_{GS2}} = \frac{2I_{DS2}}{V_{GS2} - V_t} = \frac{2I_{DS2}}{V_{IN} - V_{DS3} - V_t} \quad (15)$$

$$\frac{g_{m2}}{I_{DS2}} = \frac{2}{V_{IN} - V_{DS3} - V_t} = gmoverId2 \quad (16)$$

For low power design, higher gmoverId is recommended. To achieve such, V_{IN} and V_{BIAS} should be optimized. Keeping the input voltage V_{IN} for M2 and bias voltage V_{BIAS} at minimum will increase the efficiency of the transistors in terms of gmoverId. With this, there is a limit in the effectiveness of optimizing the input voltage V_{IN} and bias voltage V_{BIAS} to maximize the efficiency in terms of gmoverId. Lowering the drain current I_{DS} would also mean lowering gm to maintain the efficiency for low power consumption. Also, V_{IN} should be equal to V_{BIAS} to have the same $V_{GS} - V_t$ value for the two transistors, and to have a balanced gain for the two outputs RFout1 and RFout2 with respect to the input signal RFin.

I_{DS} dictates the transistor gate width (W). Increasing the supply current will require larger transistor width. Larger W would result to a larger transistor gate area which in turn increases the parasitic capacitances. Thus, design tradeoff for supply current I_{DS} and transistor sizing is inevitable.

Transistor dimensions, particularly the transistor gate width W, could be approximated with drain-to-source voltage V_{DS3} of M3 set to V_{OV} with 200mV. With V_t = 400mV, V_{DD} = 1V, transistor length L=100nm, μ = 600cm2/Vs, C_{ox} = 8.8fF/μm^2, λ = 0.1V-1, and assuming V_{IN} = 0.8V, V_{BIAS} = 0.8V, V1 = 0.7V, and V2 = 0.7V, transistor width for each branch could be extracted as

$$I_{DS1} = \frac{\mu C_{ox}}{2}\frac{W1}{L}[(V_{BIAS} - V_{DS3}) - V_t]^2[1 + \lambda(V1 - V_{DS3})] \quad (17)$$

$$W1 \approx \frac{I_{DS1}}{110.88}\ \mu m \quad (18)$$

$$I_{DS2} = \frac{\mu C_{ox}}{2}\frac{W2}{L}[(V_{IN} - V_{DS3}) - V_t]^2[1 + \lambda(V2 - V_{DS3})] \quad (19)$$

$$W2 \approx \frac{I_{DS2}}{110.88}\ \mu m \quad (20)$$

Ideally, to have a balanced output response, same amount of supply current should flow on the two branches, that is drain currents $I_{DS1} = I_{DS2}$. With the two drain currents equal, transistor width of M1 and M2 should also be equal. Note that increasing the supply current will require larger transistor width. Larger W would result to a larger transistor gate area which in turn increases the parasitic capacitances and noise. Hence, design tradeoff for drain current I_{DS} and transistor sizing is inherent.

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