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CMOS Common-Source-Drain Balun Circuit Large Signal Analysis

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I. BALUN DESIGN OVERVIEW

A balun (balanced-unbalanced) circuit converts signals that are single-ended or unbalanced with respect to ground into signals that are differential or balanced with respect to ground, and/or vice versa. An ideal balun generates a pair of differential output signals of balanced amplitudes (0 dB gain difference) and phases (180° phase shift) from a single-ended input signal source. Baluns can be classified as either active or passive baluns depending on the devices used. Active baluns, although unidirectional and more complex to implement, are preferred over their passive counterparts because they can produce gain, occupy less chip area, and can operate at higher frequencies [1-2]. One of the active balun topologies is the common-source/drain active balun circuit shown in Fig. 1.

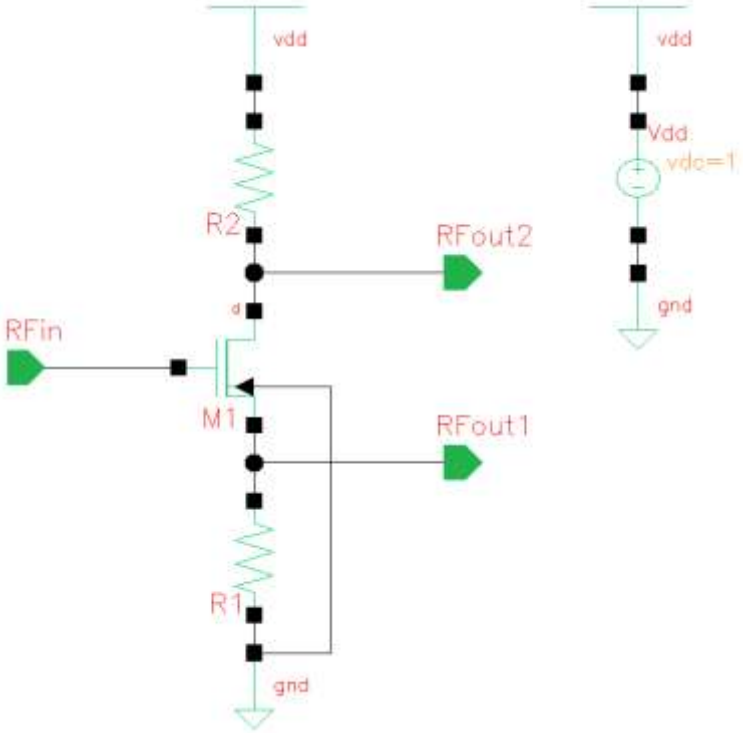

Fig. 1. Common-source/drain active balun circuit schematic.

The common-source/drain active balun is composed of just single transistor (M1) and is considered as the simplest topology amongst other active balun topologies. The input signal is fed into the gate of the transistor. Normal operation results in an inverted output signal at RFout2 and a non-inverted signal at RFout1. Ideally, these two outputs would have the same amplitude with a phase shift of 180º. Load resistors R1 and R2 determine the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

II. LARGE SIGNAL ANALYSIS

Large signal analysis or direct current (DC) analysis is critical in the design of complementary metal-oxide semiconductor (CMOS) active balun circuit as it determines the operating point and the bias conditions, and eventually large signal values are

used to find the small-signal parameters. Common-source/drain active balun is ideal for low voltage, low power radio frequency (RF) application due to low number of stacked devices. Since the two outputs should have balanced gain or attenuation, RFout2 should adjust and thus cannot produce gain. Hence, one important goal for this active balun design is to minimize the attenuation in outputs RFout1 and RFout2 and should be balanced with respect to the input signal RFin.

Drain current or drain-to-source current (I_{DS}) of transistor M1 is also the total supply current that is derived from the total power consumption of the active balun. With supply voltage V_{DD} = 1V, I_{DS} could be computed in terms of the output direct current (DC) or bias voltages V1 (or VRFout1) and V2 (or VRFout1) and the output loads R1 and R2.

$$I_{DS} = \frac{V1 - 0}{R1} = \frac{V_{DD} - V2}{R2} \quad \rightarrow \quad I_{DS} = \frac{V1}{R1} = \frac{1V - V2}{R2} \tag{1}$$

Assuming output loads R1 and R2 are equal to achieve a balanced response for V1 and V2 in terms of output swing, (1) could be expressed as

$$V1 = 1V - V2 \tag{2}$$

From the expression in (1), increasing I_{DS} increases the output voltage V1, while output voltage V2 decreases with I_{DS}. To achieve the minimum attenuation, V1 and V2 should take into account the drain-to-source voltage (V_{DS}) of transistor M1. This will also maximize the output swing in RFout1 and RFout2. Ensuring that transistor M1 operates at saturation region, V_{DS} should be at least V_{DSAT} or the overdrive voltage (V_{OV}). With supply voltage V_{DD} = 1V, V_{OV} set to 200mV and with the two outputs balanced, output voltage swings are computed as

$$V_{DS} = V2 - V1 \geq V_{DSAT} \quad \rightarrow \quad V2 - V1 \geq 0.2V \tag{3}$$

Substituting V1 expression in (2) into (3),

$$V2 - (1V - V2) \geq 0.2V \tag{4}$$

$$V2 \geq 0.6V \quad \rightarrow \quad 1V > V2 \geq 0.6V \tag{5}$$

Output DC voltage V2 is computed to swing from 0.6V to 1V. Now, calculating for the output swing for V1,

$$V2 - V1 = V_{DS,Q} \geq 0.2V \quad \rightarrow \quad V1 \leq V2 - 0.2V \tag{6}$$

$$V1 \leq 0.6V - 0.2V \tag{7}$$

$$V1 \leq 0.4V \quad \rightarrow \quad 0.4V \geq V1 > 0 \tag{8}$$

Output DC voltage swing for V1 is calculated to range from 0V to 0.4V. As previously mentioned, V1 increases with I_{DS} while V2 decreases with I_{DS}. To maximize the output swing in RFout1 and RFout2, output DC voltages V1 and V2 should have values median to their output range in (8) and (5), respectively. This would also safeguard transistor M1 to operate at saturation region with V_{DS} of at least 200mV, while varying I_{DS}. The optimized values for output DC voltages V1 and V2 are given as

$$V1 = 0.2V \tag{9}$$

$$V2 = 0.8V \tag{10}$$

With threshold voltage (V_t) set to 400mV, V_{OV} set to 200mV, V1 set to 0.2V, and $V_{DS} \geq VD_{SAT} = V_{OV}$, input bias voltage could be determined.

$$V_{DS} = V_{GS} - V_t \geq V_{DSAT} \quad \rightarrow \quad (V_{IN} - 0.2V) - 0.4V = 0.2V \tag{11}$$

$$V_{IN} = 0.8V \tag{12}$$

With input DC voltage (V_{IN}) set to 0.8V, it could swing from maximum 1V to 0.6V. Maximum input voltage is set to align with the supply voltage (V_{DD}) which is at 1V.

Drain current (I_{DS}) of transistor M1 is also the total current that is derived from the total power consumption of the active balun. Using the square-law equation for the I_{DS} in (13), transconductance (g_m) could be computed.

$$I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \tag{13}$$

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_t)(1 + \lambda V_{DS}) \tag{14}$$

$$g_m = \mu C_{ox} \frac{W}{L} (V_{IN} - V_t - V1)(1 + \lambda V_{DS}) \tag{15}$$

Substituting I_{DS} from (13) into g_m in (14),

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \frac{2I_{DS}}{(V_{GS} - V_t)} = \frac{2I_{DS}}{V_{OV}} = \frac{2I_{DS}}{V^*} = \frac{2I_{DS}}{(V_{IN} - V1 - V_t)} \quad (16)$$

$$\frac{g_m}{I_{DS}} = gmoverId = \frac{2}{(V_{IN} - V_t - I_{DS}R1)} \quad (17)$$

Proper DC input bias should be observed to realize good efficiency in terms of gmoverId. It can also be observed that the gmoverId is affected by the load resistance R1. For low power design, higher gmoverId is recommended [2-3]. As initially assumed, V_{OV} is set 200mV for minimum attenuation and/or maximum voltage swing in outputs RFout1 and RFout2 with respect to the input signal RFin. With this, circuit efficiency gmoverId could be estimated as

$$\frac{g_m}{I_{DS}} = \frac{2}{200mV} = 10V^{-1} \quad (18)$$

It can be noted that to maintain the efficiency for low power consumption, lowering I_{DS} would also mean lowering g_m. Transistor sizing depends on the target power consumption and likewise I_{DS}, thus, affecting g_m. Transconductance (g_m) is a key parameter that eventually determines the voltage gain of the active balun.

Resistors R1 and R2 could be determined given the setup for minimum attenuation and maximum voltage swing in the two outputs.

$$R1 = \frac{V1}{I_{DS}} = \frac{0.2V}{I_{DS}} \quad R2 = \frac{V_{DD} - V2}{I_{DS}} = \frac{0.2V}{I_{DS}} \quad (19)$$

To have a balanced attenuation in the two outputs, R1 should be equal to R2. With V1 and V2 set to the optimum value and V_{DD} set to 1V, decreasing the supply current (which is equal to I_{DS}) would increase the value of R1 and R2. Large resistor values contribute to more noise and parasitics. Since the active balun is targeted for low power consumption, tradeoff between drain current I_{DS} and resistor values is inevitable.

Transistor dimensions, particularly the transistor gate width (W), could be approximated with values inputted in the square-law model in (13) or in the expanded expression in (20).

$$I_{DS} = \frac{\mu C_{ox}}{2}\frac{W}{L}[(V_{IN} - V1) - V_t]^2[1 + \lambda(V2 - V1)] \quad (20)$$

Supply current (I_{DS}) dictates the transistor gate width (W). Increasing the supply current will require larger transistor width. As mentioned in the earlier section, larger W would result to a larger transistor gate area which in turn increases the parasitic capacitances and noise. Thus, design tradeoff for supply current I_{DS} and transistor sizing is also inherent.

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REFERENCES

[1] K. Jung, W.R. Eisenstadt, R.M. Fox, A.W. Ogden, and J. Yoon, "Broadband active balun using combined cascode-cascade configuration," IEEE Transactions on Microwave Theory and Techniques, vol. 56, issue 8, pp. 1790-1796, August 2008.
[2] F.R. Gomez, M.T. De Leon, and C.R. Roque, Active balun circuits for WiMAX receiver front-end, TENCON 2010 – IEEE Region 10 Conference, pp. 1156-1161, November 2010.
[3] M.E. Goldfarb, J.B. Cole, and A. Platzker, "A novel MMIC biphase modulator with variable gain using enhancement-mode FETs suitable for 3 V wireless applications," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 99-102, May 1994.
[4] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.J. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed., New York: John Wiley & Sons, Inc., 2001.
[5] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.
[6] C. Bowick, RF Circuit Design, 1st ed., USA: Howard W. Sams & Co. Inc., 1982.
[7] R.J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., New Jersey: IEEE Press, 2010, New Jersey: John Wiley & Sons, Inc., 2010.
[8] B. Razavi, RF Microelectronics, 2nd ed., Upper Saddle River, New Jersey, USA: Prentice Hall Press, 2011.
[9] F.R. Gomez, M.T. De Leon, and J.R. Hizon, Design of common-source/drain active balun using 90nm CMOS technology, Journal of Engineering Research and Reports, vol. 4, no. 3, pp. 1-9, April 2019.
[10] Cadence Design Systems, Inc. Custom IC / analog / RF design – circuit design. https://www.cadence.com/content/cadence-www/global/en_US/home/tools/custom-ic-analog-rf-design/circuit-design.html