International Journal of Scientific Engineering and Science
Volume 3, Issue 7, pp. 46-51, 2019. ISSN (Online): 2456-7361

Small-Signal Analysis of Common-Source/Drain Active Balun for RF Applications

Frederick Ray I. Gomez[1,2], Maria Theresa G. De Leon[1], John Richard E. Hizon[1]
[1]Microelectronics and Microprocessors Laboratory, University of the Philippines, Diliman, Quezon City, Philippines 1101
[2]Central Engineering & Development – NPI, STMicroelectronics, Inc., Calamba City, Laguna, Philippines 4027

Keywords— *Common-source/drain active balun; small-signal analysis; RF.*

I. OVERVIEW

The common-source/drain active balun is composed of just single transistor M1 as shown in Fig. 1 and is considered as the simplest topology amongst other active balun configurations. The input signal is fed into the gate of the transistor. Normal operation results in an inverted output signal at RFout2 and a non-inverted signal at RFout1. Ideally, these two outputs would have the same amplitude with a phase difference of 180º. Load resistors R1 and R2 determine the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

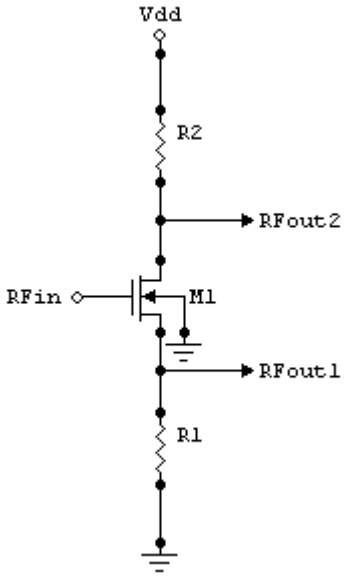

Fig. 1. Schematic diagram of common-source/drain active balun.

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. Common-drain topology or source-follower, on the other hand, is occasionally employed as level shifters or buffers, impacting the overall frequency response. It also exhibits high input impedance. With the two topologies merged to function as an active balun, common-drain will dominate the response on the overall voltage gain or attenuation because of the feedback effect of load resistor R1 with respect to the input.

II. SMALL-SIGNAL ANALYSIS

It is important to analyze the alternating current (AC) response or frequency response of the active balun to determine maximum frequency of operation and the effective bandwidth of the designed circuit. This is to ensure that the designed active balun would normally produce gain or attenuation at the desired frequency of operation, which is at 5.8GHz.

Shown in Fig. 2 is the common-source/drain high frequency small-signal equivalent circuit driven by a finite source resistance (Rs). Inherent capacitances are identified, with parasitic capacitances C_{sb} and C_{db} integrated into load capacitances C1 and C2, respectively.

International Journal of Scientific Engineering and Science
Volume 3, Issue 7, pp. 46-51, 2019. ISSN (Online): 2456-7361

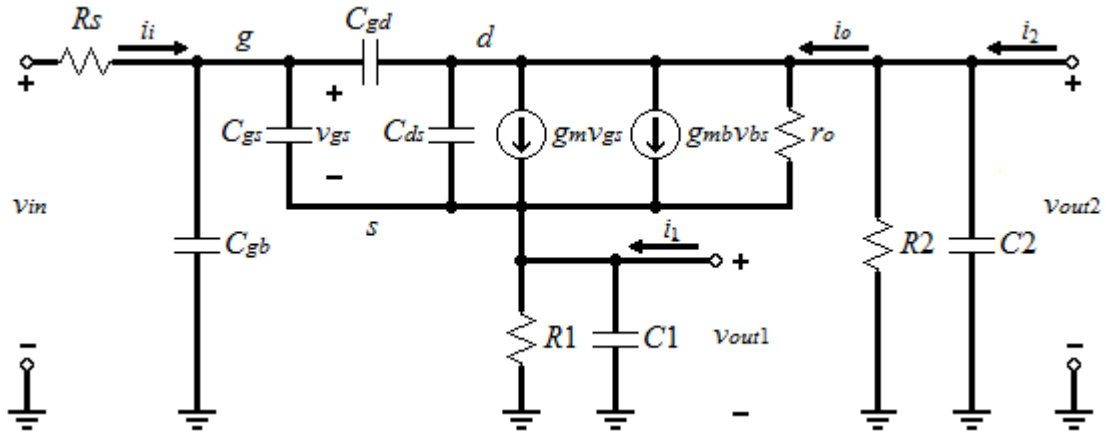

Fig. 2. Common-source/drain active balun high frequency small-signal circuit.

The bulk is assumed to be connected to the lowest power-supply voltage, which is the ground. Therefore, the bulk voltage (v_b) is constant and equal to zero. As a result, v_{bs} (not shown) changes when the output changes because the source node in connected to V1 or the RFout1, and the g_{mb} generator is active in general.

Obtaining the exact transfer function is necessary to determine the poles and estimate the effective frequency of operation of the active balun from KVL around the input loop, with Rs shorted to let $v_g = v_{in}$,

$$v_{in} = v_{gs} + v_{out1} \tag{1}$$

With the output RFout1 open circuited, $i_1 = 0$, and doing KCL at node s,

$$g_m v_{gs} + g_{mb} v_{bs} - \frac{v_{out1}}{R1 || {}^{1}/_{sC1}} + \frac{v_{out2} - v_{out1}}{r_o} = 0 \tag{2}$$

With $v_b = 0$, $v_s = v_{out1}$, and drain-to-source resistance (r_o) → ∞, (2) becomes

$$g_m (v_{in} - v_{out1}) - g_{mb} v_{out1} - \frac{v_{out1}}{R1 || {}^{1}/_{sC1}} = 0 \tag{3}$$

$$g_m v_{in} = v_{out1} \left(g_m + g_{mb} + \frac{1 + sC1R1}{R1} \right) \tag{4}$$

Voltage gain for RFout1 could now be determined.

$$A_{v1} = \frac{v_{out1}}{v_{in}}(s) = \frac{g_m}{g_m + g_{mb} + \frac{1 + sC1R1}{R1}} \tag{5}$$

$$A_{v1} = \frac{v_{out1}}{v_{in}}(s) = \frac{g_m R1}{1 + (g_m + g_{mb})R1 + sC1R1} \tag{6}$$

Voltage gain Av1 depends on the load resistor R1 as well as on the effective transconductance of the transistor. Increasing R1 with constant current would increase the source voltage or the voltage drop in R1, therefore, increasing threshold voltage (V_t) of the transistor. The change in threshold voltage is due to the body effect which is inherent when the voltage between the source and the substrate or bulk (V_{sb}) is not zero. This could affect the condition for saturation and the voltage headroom of the transistor. Hence, there is a limit in the effectiveness of increasing R1 to improve the voltage gain Av1.

From the expression in (6), the pole could be determined as

$$\omega_{p,v1} = \frac{1 + (g_m + g_{mb})R1}{C1R1} = \frac{g_m + g_{mb} + \frac{1}{R1}}{C1} \tag{7}$$

Assuming 1/R1 negligible, the pole could be approximated to be

$$f_{p,v1} = \frac{\omega_{p,v1}}{2\pi} \approx \frac{1}{2\pi} \cdot \frac{g_m + g_{mb}}{C1} \tag{8}$$

The pole is dependent on the effective transconductance of the transistor and the output load capacitance. To maximize the bandwidth, load capacitance C1 should be minimized and the transconductance g_m should be increased. With $g_m + g_{mb}$ = 22mS and load capacitance C1 = 33.33fF derived from W/L = 40µm/0.1µm of succeeding circuit block which is the mixer, the pole could be estimated as

$$f_{p,v1} \approx \frac{1}{2\pi} \cdot \frac{g_m + g_{mb}}{C1} = \frac{1}{2\pi} \cdot \frac{22mS}{33.33fF} = 105.05GHz \tag{9}$$

For the other output part, deriving the transfer function of v_{out2} with respect to v_{in}, KCL is done at node s with output RFout2 open circuited, $i_2 = 0$.

$$\frac{v_s}{R1 || {}^{1}/_{sC1}} + \frac{v_s}{r_o} = g_m(v_g - v_s) - g_{mb}v_s \tag{10}$$

Substituting $v_g = v_{in}$ with Rs = 0, and $r_o \rightarrow \infty$,

$$\frac{v_s}{R1 || {}^{1}/_{sC1}} = g_m v_{in} - (g_m + g_{mb})v_s \tag{11}$$

$$v_s\left(\frac{1 + sC1R1}{R1} + g_m + g_{mb}\right) = g_m v_{in} \tag{12}$$

$$v_s = v_{in}\frac{g_m R1}{1 + (g_m + g_{mb})R1 + sC1R1} \tag{13}$$

From KCL at node d with R2 shorted,

$$i_o + \frac{v_s}{r_o} = g_m(v_g - v_s) - g_{mb}v_s \tag{14}$$

$$i_o + \frac{v_s}{r_o} = g_m v_{in} - (g_m + g_{mb})v_s \tag{15}$$

Substituting v_s from (13) into (15), and $r_o \rightarrow \infty$,

$$i_o = g_m v_{in} - (g_m + g_{mb})\left[v_{in}\frac{g_m R1}{1 + (g_m + g_{mb})R1 + sC1R1}\right] \tag{16}$$

$$i_o = v_{in}\left[g_m - \frac{(g_m + g_{mb})g_m R1}{1 + (g_m + g_{mb})R1 + sC1R1}\right] \tag{17}$$

Solving for the equivalent transconductance G_m,

$$G_m = \frac{i_o}{v_{in}} = g_m - \frac{(g_m + g_{mb})g_m R1}{1 + (g_m + g_{mb})R1 + sC1R1} \tag{18}$$

$$G_m = \frac{i_o}{v_{in}} = \frac{g_m(1 + sC1R1)}{1 + (g_m + g_{mb})R1 + sC1R1} \tag{19}$$

Volume 3, Issue 7, pp. 46-51, 2019. ISSN (Online): 2456-7361

To compute for the voltage gain Av2 of RFout2, that is v_{out2} with respect to v_{in},

$$A_{v2} = \frac{v_{out2}}{v_{in}}(s) = -G_m \cdot R2 || {}^{1}/_{sC2} \tag{20}$$

$$A_{v2} = \frac{v_{out2}}{v_{in}}(s) = -\frac{g_m(1+sC1R1)}{1+(g_m+g_{mb})R1+sC1R1} \cdot \frac{R2}{1+sC2R2} \tag{21}$$

$$A_{v2} = \frac{v_{out2}}{v_{in}}(s) = \frac{-g_m R2}{1+(g_m+g_{mb})R1+sC1R1}\left(\frac{1+sC1R1}{1+sC2R2}\right) \tag{22}$$

Expanding (22),

$$A_{v2} = \frac{v_{out2}}{v_{in}}(s) = \frac{-g_m R2(1+sC1R1)}{\begin{array}{c}1+(g_m+g_{mb})R1+sC1R1+sC2R2 \\ +(g_m+g_{mb})sC2R2R1+sC1R1 \cdot sC2R2\end{array}} \tag{23}$$

$$A_{v2} = \frac{v_{out2}}{v_{in}}(s) = \frac{-g_m R2(1+sC1R1)}{\begin{array}{c}1+(g_m+g_{mb})R1+ \\ s[C1R1+C2R2+(g_m+g_{mb})C2R2R1]+ \\ s^2(C1R1+C2R2)\end{array}} \tag{24}$$

Voltage gain Av2 could be simplified as,

$$A_{v2} = \frac{v_{out2}}{v_{in}}(s) = \frac{-g_m R2(1+sC1R1)}{1+(g_m+g_{mb})R1+sY+s^2Z} \tag{25}$$

Where

$$Y = C1R1 + C2R2 + (g_m + g_{mb})C2R2R1 \tag{26}$$

$$Z = C1R1 + C2R2 \tag{27}$$

It can be observed that Av2 depends on the resistors R1 and R2 and also on the effective transconductance $g_m + g_{mb}$ of the transistor. The bulk or body transconductance (g_{mb}) is typically 0.1 to 0.3 times the value of g_m. It can be noted that the transfer function is of second order with dominant capacitors, C1 and C2. From the expressions in (24-25), the pole could be solved by quadratic formula, or could be estimated at

$$\omega_{p,v2} = \frac{1+(g_m+g_{mb})R1}{C1R1+C2R2+(g_m+g_{mb})C2R2R1} \tag{28}$$

$$\omega_{p,v2} = \frac{(g_m+g_{mb})+\frac{1}{R1}}{C1+C2\frac{R2}{R1}+(g_m+g_{mb})C2R2} \tag{29}$$

Assuming 1/R1 negligible, with $(g_m + g_{mb})$*C2*R2 << 1, and R1 ≈ R2, the pole could be approximated to be

$$f_{p,v2} = \frac{\omega_{p,v2}}{2\pi} \approx \frac{1}{2\pi} \cdot \frac{g_m+g_{mb}}{C1+C2} \tag{30}$$

The pole is dependent on the effective transconductance of the transistor and the output load capacitances. To maximize the bandwidth, load capacitances C1 and C2 should be minimized and the transconductance g_m should be increased.

With $g_m + g_{mb}$ = 22mS and load capacitances C1 = 33.33fF and C2 = 33.33fF, the pole could be estimated as

$$f_{p,v2} \approx \frac{1}{2\pi} \cdot \frac{g_m + g_{mb}}{C1 + C2} = \frac{1}{2\pi} \cdot \frac{22mS}{66.66fF} = 52.53GHz \tag{31}$$

Letting s = 0, voltage gains Av1 and Av2 from (6) and (25), respectively, could be estimated or simplified. This also neglects the effects of the capacitances in the circuit. Shown in Fig. 3 is the common-source/drain active balun small-signal simplified model. It is also noted that input of the common-source/drain active balun is connected to the gate of transistor M1, thus input resistance (R_i) → ∞.

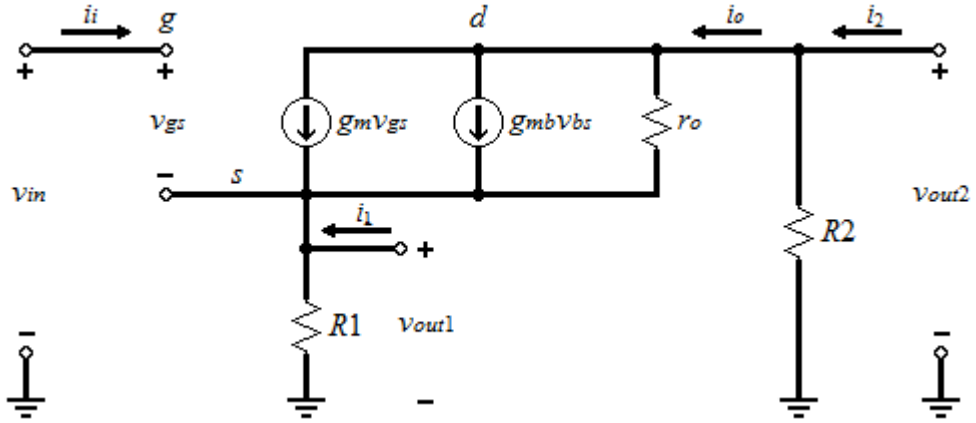

Fig. 3. Common-source/drain active balun low frequency small-signal circuit.

Voltage gains Av1 and Av2 could be simplified as follows:

$$A_{v1} = \frac{v_{out1}}{v_{in}} = \frac{g_m R1}{1 + (g_m + g_{mb})R1} \tag{32}$$

$$A_{v2} = \frac{v_{out2}}{v_{in}} = \frac{-g_m R2}{1 + (g_m + g_{mb})R1} \tag{33}$$

As illustrated, Av1 depends on output load R1 and effective transconductance $g_m + g_{mb}$ of the transistor, and Av2 depends on the resistors R1 and R2 and $g_m + g_{mb}$ of the transistor. Equating the two equations of voltage gains in (32) and (33) in order to have a balanced gain or attenuation in the two outputs, R2 should be equal to R1. It would then be necessary to determine the proper value for R1 = R2 to minimize the attenuation of the two outputs with respect to the input, with all other conditions taken into account for the circuit design. Also worth noting is that increasing R1 with constant current would increase the source voltage or the voltage drop in R1, therefore increasing threshold voltage (V_t) of the transistor. The change in threshold voltage is due to the body effect which is inherent when the voltage between the source and the substrate or bulk (V_{sb}) is not zero. This could affect the condition for saturation and the voltage headroom of the transistor. Hence, there is a limit in the effectiveness of increasing R1 to improve the voltage gains Av1 and Av2.

Although common-source-drain active balun has a simple topology, tradeoffs in device parameters are inevitable in attaining the balanced gain for the two output nodes. From (32) and (33) for Av1 and Av2, g_{mb} assumed to be $0.1g_m$, r_o neglected, and with the equation for $g_m$overI_d and R1, the minimum balanced attenuation could be estimated as

$$|A_{v1}| = \left|\frac{v_{out1}}{v_{in}}\right| = \frac{g_m R1}{1 + (g_m + g_{mb})R1} \approx \frac{g_m \frac{0.2V}{I_{DS}}}{1 + 1.1 \cdot g_m \frac{0.2V}{I_{DS}}} \tag{34}$$

$$|A_{v1}| = \left|\frac{v_{out1}}{v_{in}}\right| \approx \frac{\left(\frac{2}{0.2V}\right)0.2V}{1 + 1.1\left(\frac{2}{0.2V}\right)0.2V} = \frac{2}{3.2} \tag{35}$$

$$|A_{v1}| = \left|\frac{v_{out1}}{v_{in}}\right| \approx 0.625 \tag{36}$$

To approximate the value of the resistors R1and R2, computed value for the voltage gain expressions in (32-33) could be used. Setting |Av1| = |Av2| = 0.5,

$$R1 \approx R2 = \frac{|A_{v1,2}|}{g_m(1 - 1.1 \cdot |A_{v1,2}|)} = \frac{0.5}{g_m[1 - 1.1(0.5)]} = \frac{1.111}{g_m} \quad (37)$$

Substituting g_m in terms of I_{DS} with V_{OV} = 200mV, resistors R1 and R2 become

$$R1 \approx R2 = \frac{1.111 \cdot V_{OV}}{2I_{DS}} = \frac{1.111(0.2V)}{2I_{DS}} = \frac{0.111V}{I_{DS}} \quad (38)$$

For low power design, tradeoff between the supply current and resistor values is unavoidable. Voltage gain performance would also be affected with changes in I_{DS}. With low supply current, voltage attenuation could be minimized by increasing the resistor value. As the resistor value goes high, the voltage gain approaches unity. But increasing the resistor value would also contribute to larger noise and more parasitics. Lower resistor value increases the cutoff frequency or the pole location, and the circuit bandwidth, consequently. With this, there is a limit in the effectiveness of optimizing the supply current and the output loads to minimize noise, minimize power consumption, increase the circuit bandwidth, and improve the voltage gain performance of the active balun design.

Transconductance g_m of the transistor is affected by the transistor width size W. Increasing g_m also increases the cutoff frequency (f_T), hence transistor sizing directly affects the f_T performance or the circuit bandwidth. However, larger W means more chip area which in turn increases the parasitic capacitances. At higher frequencies, the parasitic capacitances present a low-impedance path to the radio frequency (RF) signals causing the deviation in the ideal operation of the transistor. This will affect the performance of the transistor when amplifying signals at high frequencies. In addition, increasing g_m with W contributes more noise to the circuit, which will be discussed on a separate paper.

ACKNOWLEDGMENT

The authors would like to share the appreciation to the Department of Science and Technology (DOST), the Philippine Council for Advanced Science and Technology Research and Development of DOST (DOST-PCASTRD), and the Engineering Research and Development for Technology Consortium (DOST-ERDT) for the extensive support. The authors would also like to thank the Microelectronics and Microprocessors Laboratory team of the University of the Philippines for the technical support during the course of the study. Author F.R. Gomez would like to extend gratitude to the STMicroelectronics Calamba Central Engineering and Development Team and the Management Team for the great support.

REFERENCES

[1] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.J. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed., New York: John Wiley & Sons, Inc., 2001.
[2] C. Bowick, RF Circuit Design, 1st ed., USA: Howard W. Sams & Co. Inc., 1982.
[3] R.J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., New Jersey: IEEE Press, 2010, New Jersey: John Wiley & Sons, Inc., 2010.
[4] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.
[5] F.R. Gomez, M.T. De Leon, and C.R. Roque, Active balun circuits for WiMAX receiver front-end, TENCON 2010 – IEEE Region 10 Conference, pp. 1156-1161, November 2010.
[6] F.R. Gomez, M.T. De Leon, and J.R. Hizon, Design of common-source/drain active balun using 90nm CMOS technology, Journal of Engineering Research and Reports, vol. 4, no. 3, pp. 1-9, April 2019.
[7] Cadence, LNA design using SpectreRF, Application Note, product version 6.0, November 2005.
[8] Cadence, Mixer Design Using SpectreRF, Application Note, product version 5.0, June 2004.