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Common-Gate with Common-Source Active Balun Circuit Small-Signal Analysis in CMOS Technology

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I. Active Balun Circuit Overview

This active balun is comprised of 2 amplifiers namely common-gate (CG) amplifier (M1) in the 1st stage and common-source (CS) amplifier (M2) in the 2nd stage as shown in the Fig. 1. The input signal is fed into the drain of M1 and into the gate of M2, while the outputs are probed at the drains of M1 and M2. Load resistors R1 and R2 dictate the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

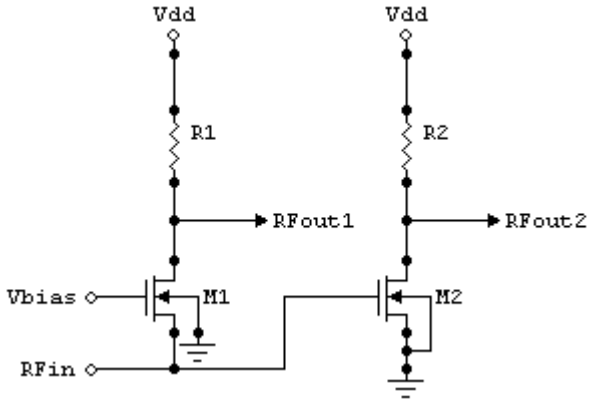

Fig. 1. Common-gate with common-source active balun circuit schematic.

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. With this, it finds wide applications in analog circuits and its frequency response is of interest. Common-gate topology exhibits no Miller multiplication of capacitances, potentially achieving a wide band [1-2]. However, the low input impedance may load the preceding stage. Furthermore, since the voltage drop across load or output resistor R1 is typically maximized to obtain the required gain, the direct current (DC) level of the input signal must be quite low. With the two topologies cascaded to function as an active balun, one major challenge would be to generate balanced gain for the two outputs RFout1 and RFout2 with respect to the input signal RFin, given that the input signal is fed into two different transistor ports.

II. Small-Signal Analysis

It is important to analyze the alternating current (AC) response or frequency response of the active balun to determine maximum frequency of operation and the effective bandwidth of the designed circuit. This is to ensure that the designed active balun would normally produce gain or attenuation at the desired frequency of operation, implemented in a complementary metal-oxide semiconductor (CMOS) technology.

The small-signal analysis of the common-gate with common-source active balun can be subdivided into two – the analysis of common-gate (CG) stage and common-source (CS) stage. Shown in Fig. 2 is the hybrid-π model of CG amplifier, and Fig. 3 shows the conversion into the equivalent T-model.

The two dependent sources in Fig. 2 can be combined into one current source assuming that the bulk or substrate connection operates at ac ground. And given that the gate also operates at ac ground, v_{bs} will then be equal to v_{gs}. This combined current source $(g_m + g_{mb})*v_{gs}$ can be replaced by two current sources which are actually equal: one from the source to the gate and one from the gate to the drain. Since the current source flowing from the source to the gate is controlled by v_{sg} itself, applying Ohm's law would result to resistor of value $1/(g_m + g_{mb})$ as shown in Fig. 3. This value is the input resistance (R_{in1}) of the CG amplifier.

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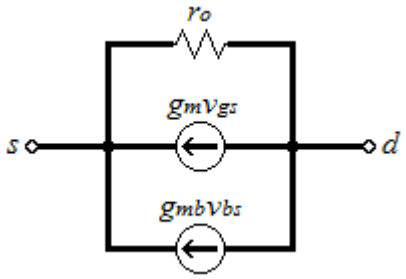

Fig. 2. Common-gate small-signal simplified low frequency hybrid-pi model.

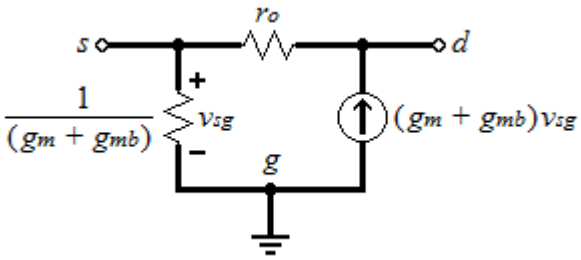

Fig. 3. Equivalent common-gate small-signal T-model.

$$R_{in1} = \frac{v_i}{i_i} = \frac{v_{sg}}{(g_{m1} + g_{mb1})v_{sg}} = \frac{1}{g_{m1} + g_{mb1}} \tag{1}$$

Using the T-model and with r_o assumed negligible, the small-signal equivalent circuit of the common-gate stage with source resistance (Rs), parasitic capacitances, and load resistance R1 is shown in Fig. 4 below. Output capacitance C1 is integrated with the effective capacitance at node d (C_d).

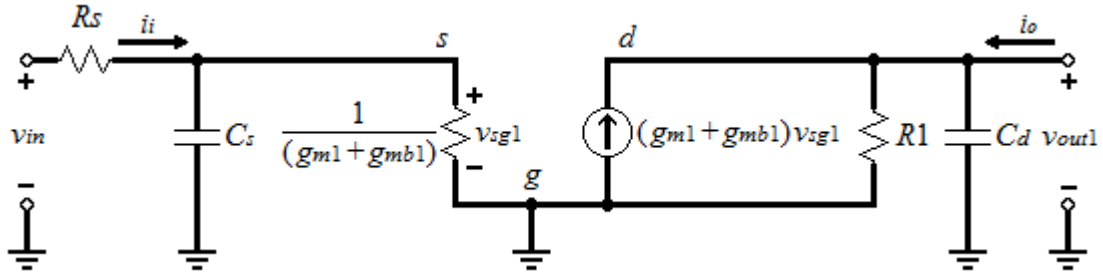

Fig. 4. Common-gate high frequency small-signal model.

The capacitances contributed by the transistor are connected from the input and output nodes to ground. At node s, effective capacitance $C_s = C_{sg1} + C_{sb1}$, yielding a pole frequency of

$$\omega_{in1} = \frac{1}{R_{in,eff} \cdot C_{in,eff}} = \frac{1}{(R_{in1} || Rs) C_s} = \frac{g_{m1} + g_{mb1} + \frac{1}{Rs}}{C_{sg1} + C_{sb1}} \tag{2}$$

Correspondingly, at node d, effective capacitance $C_d = C_{dg1} + C_{db1} + C1$ giving a pole frequency of

$$\omega_{out1} = \frac{1}{R_{out,eff} \cdot C_{out,eff}} = \frac{1}{R1 \cdot C_d} = \frac{1}{R1\left(C_{dg1} + C_{db1} + C1\right)} \tag{3}$$

The overall transfer function is thus given by the succeeding equation. The first fraction represents the low-frequency gain of the common-gate circuit. Drain-to-source resistance r_{o1} is assumed to be negligible. Note that if r_{o1} is not omitted, the input and output nodes interact thus making it difficult to calculate for the poles [1-3].

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$$A_{v1} = \frac{v_{out1}}{v_{in1}}(s) = \frac{(g_{m1} + g_{mb1})R1}{1 + (g_{m1} + g_{mb1})Rs} \cdot \frac{1}{\left(1 + \frac{s}{\omega_{in1}}\right)\left(1 + \frac{s}{\omega_{out1}}\right)} \tag{4}$$

$$A_{v1} = \frac{(g_{m1} + g_{mb1})R1}{1 + (g_{m1} + g_{mb1})Rs} \cdot \left(\frac{1}{1 + \frac{C_{sg1} + C_{sb1}}{g_{m1} + g_{mb1} + \frac{1}{Rs}} s} \right) \cdot \left[\frac{1}{1 + R1(C_{dg1} + C_{db1} + C1)s} \right] \tag{5}$$

For the common-source stage with the RFout2 branch, the output pole could be derived from the active balun discussion in [4] and in the discussion of the common-gate part. To summarize the transfer function for A_{v2},

$$A_{v2} = \frac{v_{out2}}{v_{in2}}(s) = \frac{-g_m R2}{\left(1 + \frac{s}{\omega_{in2}}\right)\left(1 + \frac{s}{\omega_{out2}}\right)} \tag{6}$$

Where

$$\omega_{in2} = \frac{1}{Rs\left[C_{gs2} + (1 + g_m R2)C_{gd2}\right]} \tag{7}$$

$$\omega_{out2} = \frac{1}{R2\left(C_{gd2} + C_{db2} + C2\right)} \tag{8}$$

Since the common-source stage shares the same input node as the common-gate stage, one input pole will dominate the other. Between the two stages and based on their equation on the input pole, common-gate stage will have the smaller bandwidth and thus dominates the overall input pole of the active balun.

Solving for the voltage gains at DC and/or low frequency, capacitances are omitted. Source resistance (Rs) is shared for both the inputs of the common-gate branch and the common-source branch. Shown in Fig. 5 to 6 are the low frequency small signal model of the common-gate stage and common-source stage, respectively. Drain-to-source resistance (r_o) is omitted in the common-gate stage to have isolation between input and output resistances.

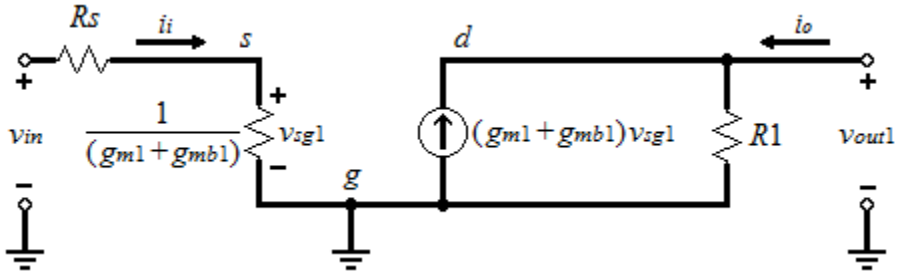

Fig. 5. Common-gate low frequency small-signal model.

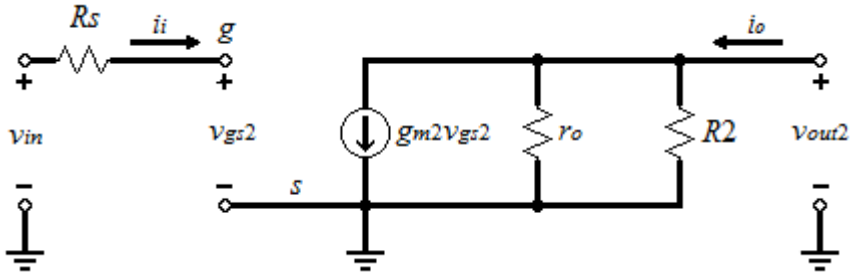

Fig. 6. Common-source low frequency small-signal model.

Voltage gains A_{v1} and A_{v2} are simplified as

$$A_{v1} = \frac{v_{out1}}{v_{in}} = \frac{(g_{m1} + g_{mb1})R1}{1 + (g_{m1} + g_{mb1})Rs} \tag{9}$$

$$A_{v2} = \frac{v_{out2}}{v_{in}} = -g_{m2}R2 \tag{10}$$

Equating the two voltage gain expressions to check the relationship and behavior of the two output stages,

$$|A_{v1}| = |A_{v2}| = \frac{(g_{m1} + g_{mb1})R1}{1 + (g_{m1} + g_{mb1})Rs} = g_{m2}R2 \tag{11}$$

Assuming $Rs = R_{in1} = 1 / (g_{m1} + g_{mb1})$,

$$|A_{v1}| = |A_{v2}| = \frac{(g_{m1}+g_{mb1})R1}{2} = g_{m2}R2 \tag{12}$$

$$R1 = \frac{2g_{m2}R2}{g_{m1}+g_{mb1}} = 2g_{m2}R2 \cdot R_{in1} \quad , \quad R2 = \frac{R1}{2g_{m2}R_{in1}} \tag{13}$$

$$Rs = R_{in1} = \frac{R1}{2g_{m2}R2} \tag{14}$$

Input resistance of the common-gate amplifier is affected by the values of resistors R1 and R2, unlike that of the common-source amplifier that has very high input impedance ideally at infinity. But when the two configurations are combined as in the case of the common-gate with common-source active balun, input resistance (R_{in1}) will also dictate the input resistance of the common-source part, thus the Rs. The effective input resistance of the active balun could be estimated as the Rs given in (14). With this, operation of the common-source part could be affected by the variation of the resistor R1 of the common-gate part, and vice versa. Increasing load resistors R1 and R2 would increase the voltage gains A_{v1} and A_{v2}, respectively. But with the power consumption requirement, there will be a limit in the effectiveness of increasing R1 and R2.

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