Noise Performance Analysis of Differential Active Balun Transformer Circuit

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I.   DIFFERENTIAL ACTIVE BALUN CIRCUIT OVERVIEW

A balun (balanced-unbalanced) circuit is a type of transformer that converts signals that are single-ended or unbalanced with respect to ground into signals that are differential or balanced with respect to ground, and vice versa. Fig. 1 illustrates a typical balun circuit that transforms signal from single-ended input voltage (Vin) into differential output voltages (V+ and V-) with half the amplitude of Vin and 180° phase difference. An ideal balun generates a pair of differential output signals of balanced amplitudes (0 dB gain difference) and phases (180° phase difference) from a single-ended input signal source.
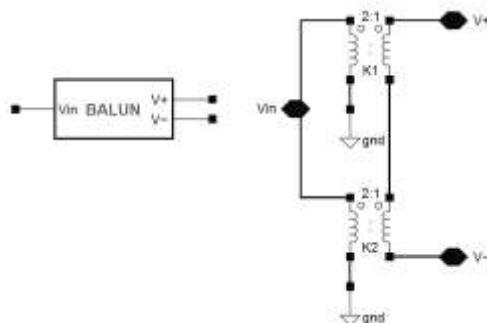

Fig. 1. Typical balun circuit.

Baluns can be classified as either active or passive baluns depending on the devices used. Active baluns, although unidirectional and more complex to implement, are preferred over their passive counterparts because they can produce gain, occupy less chip area, and can operate at higher frequencies [1-2]. One of the active balun topologies is the differential active balun transformer circuit in Fig. 2, composed of 3 transistors namely M1 and M2 for the differential output, and M3 for the tail current. The input signal is applied at the input of one of the differential pair transistors and will ideally split equally between the pair with same amplitude and 180° phase difference. Remarkably, this active balun topology is capable of producing gain.
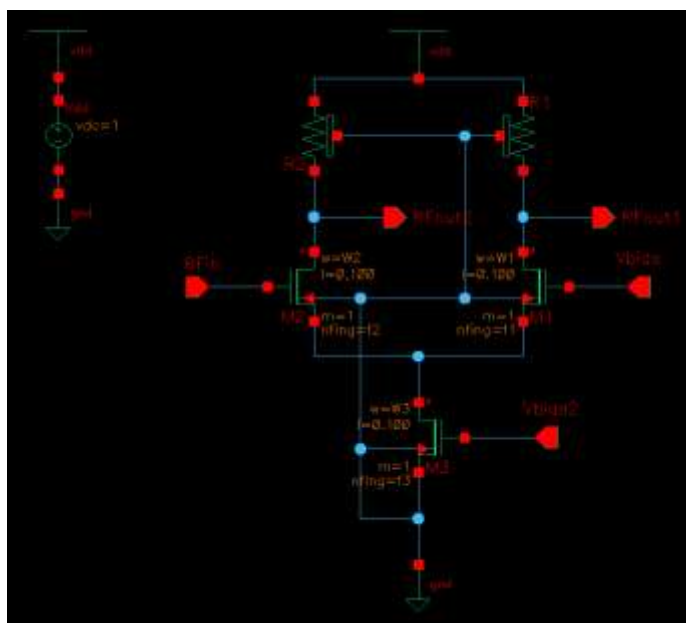

Fig. 2. Differential active balun transformer circuit schematic.

II.   Noise Performance

The very weak signal received by the radio frequency (RF) circuit makes the input signal very susceptible to noise. The existence of noise is essentially due to the fact that electrical charge is not continuous but rather carried in discrete amounts equal to the electron charge [3-4]. The study of noise is important because it represents a lower limit to the size of the electrical signal that can be amplified by the RF circuit without significantly deteriorating the signal quality. Hence it is important that each block in the RF receiver contributes as little noise as possible.

Important design parameters namely signal-to-noise ratio (SNR), dynamic range (DR), and noise figure (NF) can be derived using noise analysis. Shown in Fig. 3 is the circuit model with noise sources of differential active balun transformer circuit.
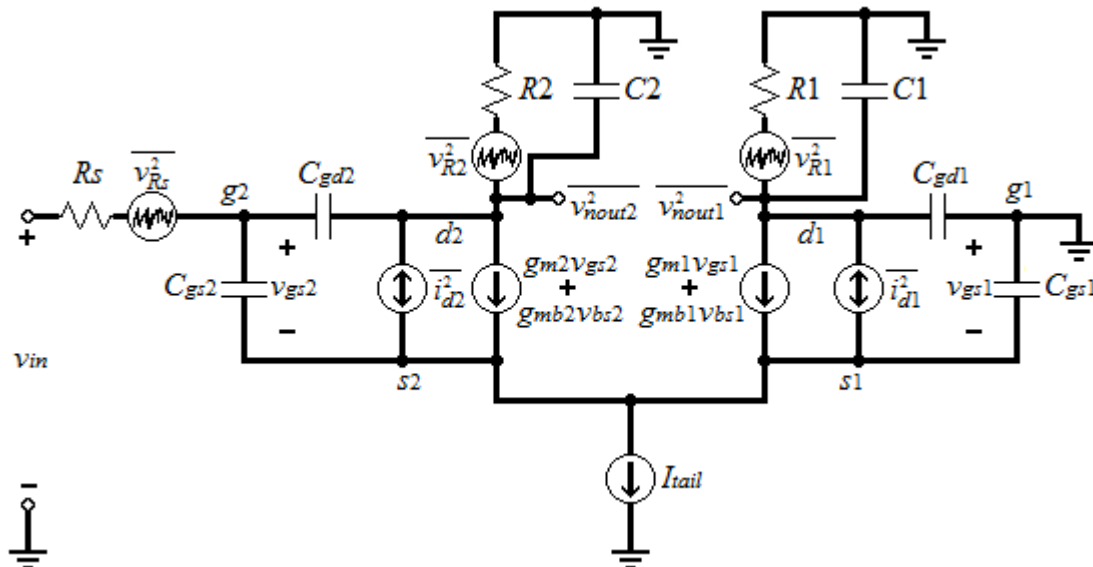

Fig. 3. Differential active balun transformer model with noise generator.

Since differential active balun supplies differential input signal into a differential circuit, noise calculation for each of the two output nodes is necessary. Starting with KCL at node d2, output noise voltage and current of RFout2 are determined in the succeeding equations.

$$\overline{i_{n,out2}^2} = \overline{i_{d2,th}^2} + \overline{i_{d2,1/f}^2} + \overline{i_{R2}^2} + \frac{\overline{v_{Rs}^2} - \overline{v_{n,out2}^2}}{\left(1/sC_{gd2}\right)^2} \tag{1}$$

$$\overline{v_{n,out2}^2} = \left[4k_BT\gamma(g_{m2} + g_{mb2})\Delta f + \frac{K_fI_{D2}}{L^2C_{ox}}\frac{1}{f_{co}}\Delta f + \frac{4k_BT}{R2}\Delta f + \frac{\overline{v_{Rs}^2} - \overline{v_{n,out2}^2}}{\left(1/sC_{gd2}\right)^2} \right]\left(R2||\frac{1}{sC2}\right)^2 \tag{2}$$

At higher frequency, thermal noise of transistor dominates, hence flicker noise could be neglected. Rearranging (2), output voltage noise of RFout2 could be simplified. With source resistance Rs assumed to be negligible,

$$\overline{v_{n,out2}^2} = \frac{k_BT}{C2} \cdot \frac{1 + \gamma(g_{m2} + g_{mb2})R2}{1 + \frac{1}{4}\left(\frac{C_{gd2}}{C2}\right)^2} \quad V_{rms}^2 \tag{3}$$

If output capacitance C2 dominates rather than the inherent C_{gd2}, (3) could then be simplified as

$$\overline{v_{n,out2}^2} = \frac{k_BT}{C2}\left[1 + \gamma(g_{m2} + g_{mb2})R2\right] \quad V_{rms}^2 \tag{4}$$

From (4), increasing the resistance R2 increases the overall noise. Output capacitance C2 dictates significantly, if compared to C_{gd2}, on the output noise performance. Increasing the capacitance would decrease the output voltage noise but it would also decrease the circuit bandwidth or the cutoff frequency of RFout2. This design tradeoff is inevitable so one should consider the effectiveness of setting or limiting the output capacitance.

For RFout1, the output noise voltage and current could be determined starting from KCL at node d1. If the circuit is symmetric, then the noise (denoted as $i_{n,tail}$) generated in I_{tail} divides equally between M1 and M2 producing only a common-mode noise voltage at the output. If the tail current noise is negligible, that is $i_{n,tail} \ll I_{tail}$, and source resistance (Rs) assumed also to be negligible, a symmetric noise equation could be achieved. Doing KCL at node s1 (or s2),

$$\overline{i_{d1,th}^2} + \overline{i_{d1,1/f}^2} = \overline{i_{d2,th}^2} + \overline{i_{d2,1/f}^2} \tag{5}$$

Output noise voltage and current for RFout1 branch could now be expressed with KCL at node d1.

$$\overline{i_{n,out1}^2} = \overline{i_{d1,th}^2} + \overline{i_{d1,1/f}^2} + \overline{i_{R1}^2} \tag{6}$$

$$\overline{v_{n,out1}^2} = \left\{ 4k_B T \left[\gamma(g_{m1} + g_{mb1}) + \frac{1}{R1} \right] + \frac{K_f I_{D1}}{L^2 C_{ox} f_{co}} \frac{1}{} \right\} \Delta f \cdot \left[\frac{R1}{R1(sC1 + sC_{gd1}) + 1} \right]^2 \tag{7}$$

Assuming flicker noise is neglected at higher frequency,

$$\overline{v_{n,out1}^2} = \frac{k_B T}{C1 + C_{gd1}} [1 + \gamma(g_{m1} + g_{mb1})R1] \tag{8}$$

If output capacitance C1 dominates the other capacitance C$_{gd1}$ (or C$_{gd1}$ assumed negligible), expression in (8) could be simplified as

$$\overline{v_{n,out1}^2} = \frac{k_B T}{C1} [1 + \gamma(g_{m1} + g_{mb1})R1] \tag{9}$$

From (9), increasing the resistance R1 increases the overall noise while increasing the load capacitance C1 decreases the circuit noise. However, increasing the capacitance C1 would also decrease the circuit bandwidth or the cutoff frequency of RFout1. This design tradeoff is inevitable so one should consider the amount of output capacitance.

Input-referred noise voltage, on the other hand, can be derived by expressing the output noise voltage with the small-signal gain. To illustrate,

$$\overline{v_{n,in}^2} = \frac{\overline{v_{n,out1}^2}}{A_{v1}^2} = \frac{\overline{v_{n,out2}^2}}{A_{v2}^2} \quad V_{rms}^2 \tag{10}$$

Using the expression for SNR given as the output noise voltage in (9) and (4), dynamic range of the circuit for the RFout1 and RFout2 side, respectively, could be determined. Dynamic range is the ratio of the maximum signal power that the circuit can tolerate without distortion to noise level of circuit. The largest signal that can be passed through the output of the circuit is limited by the supply voltage V$_{DD}$. Dynamic range is expressed as

$$DR_1 = 10 log \frac{V_{DD}^2 \cdot C1}{1 + \gamma(g_{m1} + g_{mb1})R1} + 83.828 \quad dB \qquad \text{with C1 in pF, at room temperature} \tag{11}$$

$$DR_2 = 10 log \frac{V_{DD}^2 \cdot C2}{1 + \gamma(g_{m2} + g_{mb2})R2} + 83.828 \quad dB \qquad \text{with C2 in pF, at room temperature} \tag{12}$$

Plugging in the input noise expression with input impedance (R$_i$) not equal to the source resistance (Rs), and the derived output noise contributions from (9) and (4), noise factors are computed as

$$F_{m1} = 1 + \frac{N_{m,out1}}{G_{m1} N_i} = 1 + \frac{1 + \gamma(g_{m1} + g_{mb1})R1}{C1 \cdot 4 \frac{R_S R_i}{(R_S + R_i)^2} \Delta f \cdot A_{v1}} \tag{13}$$

$$F_{m2} = 1 + \frac{N_{m,out2}}{G_{m1} N_i} = 1 + \frac{1 + \gamma(g_{m2} + g_{mb2})R2}{C2 \cdot 4 \frac{R_S R_i}{(R_S + R_i)^2} \Delta f \cdot A_{v2}} \tag{14}$$

Noise figures are then expressed as

$$NF_{m1} = 10 log \left[1 + \frac{1 + \gamma(g_{m1} + g_{mb1})R1}{C1 \cdot 4 \frac{R_S R_i}{(R_S + R_i)^2} \Delta f \cdot A_{v1}} \right] dB \tag{15}$$

$$NF_{m2} = 10 log \left[1 + \frac{1 + \gamma(g_{m2} + g_{mb2})R2}{C2 \cdot 4 \frac{R_S R_i}{(R_S + R_i)^2} \Delta f \cdot A_{v2}} \right] dB \tag{16}$$

If R$_i$ is matched with Rs, input noise (Ni) could be simplified to Ni = k$_B$TΔf. Plugging in the expressions for the voltage gains (A$_{v1}$ and A$_{v2}$), the noise factors would expand to

$$F_{m1} = 1 + \frac{1 + \gamma(g_{m1} + g_{mb1})R1}{C1 \cdot k_B T \Delta f \cdot A_{v1}} \tag{17}$$

$$F_{m1} = 1 + \frac{1 + \gamma(g_{m2} + g_{mb2})R2}{C2 \cdot k_B T \Delta f \cdot A_{v2}} \tag{18}$$

Noise figures are then computed as the following, for input impedance matched with Rs.

$$NF_{m1} = 10 \log \left[1 + \frac{1 + \gamma(g_{m1} + g_{mb1})R1}{C1 \cdot k_B T \Delta f \cdot A_{v1}} \right] \ dB \tag{19}$$

$$NF_{m2} = 10 \log \left[1 + \frac{1 + \gamma(g_{m2} + g_{mb2})R2}{C2 \cdot k_B T \Delta f \cdot A_{v2}} \right] \ dB \tag{20}$$

Noise performance is an important design consideration since it determines the vulnerability of the active balun to unwanted signal like noise. Hence it is critically important that the differential active balun transformer circuit contributes as little noise as possible in the system level design of RF applications.

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