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Systematic Approach for Simulation Based System Level Modeling

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Abstract*—System Level Modeling and Analysis is playing important role to achieve faster architecture exploration and efficient implementation. Simulation Based System Level Modeling is the better choice to achieve the faster simulation and accurate results compare to other methods. Challenges of the system level modeling needs more modeling effort and require the larger learning curve to understand the modeling concepts. Proposed work is to discuss the system level modeling concepts and demonstrating the systematic approach for system level modeling using VisualSim*. This work showcase the steps involved in modeling, starts from idea or system specification with modeling objectives to the optimized, validated and executable specification for further implementation.*

***Keywords*—** *System Level Modeling, Performance, Power, VisualSim, Simulation.*

I. INTRODUCTION

System Level Modeling is to build the complete system using abstract blocks in order to understand the system bottlenecks, feasibility of the system, and probability of a successful implementation in a cost effective manner. It is better solution for optimizing design metrics early in the design stage and to achieve faster system development.

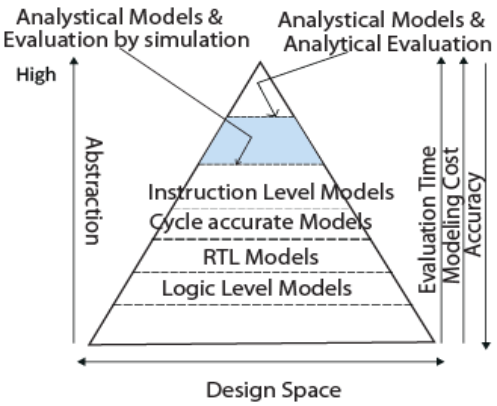

Fig. 1. Tradeoffs at various levels of abstraction.

System Level Modeling using simulation method is faster and more accurate. This method meets the identified gap as shown in the Fig. 1. Modeling using series of equations is much faster but less accurate. Modeling at lower levels of abstractions is more accurate but requires more modeling cost time. System Model can be depicted as given in equation 1.

$$SM = WM + BM + AM + MO \quad (1)$$

Where,

SM $\rightarrow$ System Model,
WM $\rightarrow$ Workload Model,
BM $\rightarrow$ Behaviour Model,
AM $\rightarrow$ Architecture Model,
MO $\rightarrow$ Modeling Objectives

System Model is the mathematical representation of the stimulus, description of the actual or theoretical physical system and the viewers for the output [1]. It consists of a Source, System, Results, Simulator and Parameters. Performance modeling is part of system level modeling in which each system components are characterized with respect to timing. Task or process execution time in the system measures the performance. Optimizing power dissipation is done by clock rate reduction; voltage reduction and cache disable instructions methods. Optimizing requirement of resources such as processors, memories, and bus is on the basis of performance and power numbers. Proposed simulation based system level modeling shows workload modeling, behaviour modeling and architecture modeling with less modeling effort in short period of time.

II. METHODOLOGY

Simulation Based System Level Modeling involves following steps.

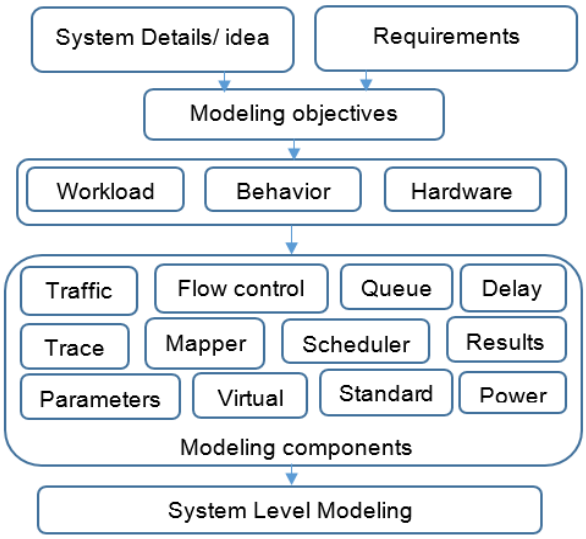

Fig. 2. System level modeling approach.

- Defining system modeling goals for given system details and requirements.

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- Describing workload which represent the stimulus or activity inputs to the system
- Describing the analysis (Performance/power) specific behavior of the system.
- Identifying the modeling components for behavior, architecture and workload.
- System modeling, Simulation, post processing,
- Analysis, optimization and validation.

Workload represents arrival of the information to the system at defined or undefined events of time. It works as stimulus to the model. Workload can be the data structure (transaction containing fields) representing video frames, signals through pins, network packets and control messages in hardware or software, sequence of reads and writes and series of activity. Arrival of the information can be modeled as a fixed sequence, distribution-based, standard defined or a traced file from an existing system. Workload Model can be depicted as.

$$WM = MO + DS + AT + TR \quad (2)$$

Where,

DS $\rightarrow$ Data Structure,

AT $\rightarrow$ Activity,

TR $\rightarrow$ Traffic.

Workload should be kept small number of operation. Too Many operations can make the workload not only difficult to construct and manage but also less useful for understanding performance. It is not necessary to simulate every single use case, rather focus on the use cases that are most likely to occur. The lower frequency one can be ignored or combined with others into a single operation [2].

The behaviour flow describes the order and dependency of the tasks that are processed on the data. The behavior can contain multiple flows that are dependent or independent. The behaviors have no notion of an implementation. In a performance model, they do contain the timing information. The actual execution of the timing is performed on the architecture. Behavior model can be expressed as

$$BM = TF + DF + TM \quad (3)$$

Where

TF $\rightarrow$ Task flow,

DF $\rightarrow$ Data flow,

TM $\rightarrow$ Task Mapping

In queuing modeling behavior of the application is characterized by queue, delay and processing models. It begins during the early phases of the application design. This is essential where mathematical analysis is not possible for complex systems such as queuing network system with complex resource scheduling algorithm and to predict the effect of contention for resources on performance. According to queuing modeling, Process is function which operates on a sequence of data elements which can be finite or infinite in length.

Architectural modeling involves the modeling of systems using performance models of processors, co-processors, memories, busses available in VisualSim libraries. Architecture models only need to account for timing behavior, Source and sink processes are mapped onto the same processing component.

AM=Resource Speed + Scheduler (4)

Hardware level models are constructed to determine the system impact of particular technology detail of the hardware then one should choose Hardware level modeling or timing accurate abstraction level. Hardware level accuracy model which is developed using prebuilt library blocks which are timing and functionally accurate. At this level of modeling there will be a very limited scope for modifying the system topology and parameterization. This level of modeling methodology will be ideal when the architecture is finalized but needs further verification of specification.

The evaluation of architecture is performed by simulating the performance consequences of the application events comparing from the application model that is mapped onto the architecture model. When executed each application process generates trace of events and these event of traces are routed toward a specific component of the architecture model a means of trace event queue.

Case study:

System consists of four tasks, each task process the data streams from source. The data streams consist of set of data tokens that are generated by data source. Data streams are processed by dedicated task on hardware and these data tokens are collected by sink. Goal of the analysis to find performance characteristics of the system such as the maximum end to end delays data tokens (latency), or maximum buffer fill levels. Queuing modeling for the given specification as shown in Fig. 3. in which each task in the system is modeled using queue and delay. Task on the hardware unit has dedicated input buffer which temporarily stores data tokens if the hardware unit already busy. Data tokens are shared or processed in a sequential manner, so hardware unit can be assigned only one token at a time. The token arrived in buffer have to wait their turn on the hardware unit.

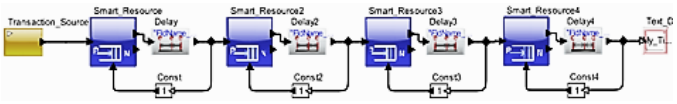

Fig. 3. Queuing modeling.

Next event in the buffer is popped up after getting completion acknowledgement from the hardware unit. Hardware scheduling for next event is considered either FIFO or priority based. Dedicated task processed on hardware unit with the execution length range between 1.0 to 3.5 units. We assume that the data generation pattern of source is fixed time distribution.

Above model can be modified to model in which hardware and behavior flow are modeled separately. This kind of modeling is useful for optimizing and validating the hardware requirements for given specification and defined metrics. Information required to model hardware component is processing speed or task relative processing time, context switching time. Information required to model behavior flow is, resource name to which task to be mapped task processing time.

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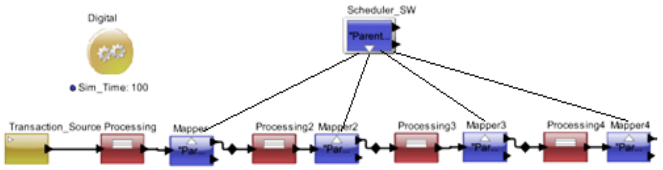

Fig. 4. Resource modeling and mapping.

In hardware modeling shows in Fig. 5, data sheet details are required to model the hardware components. Data sheet information for microprocessor is speed, size, pipelining stages, cache level, and instruction set. Software components are modeled either by cycle trace file or by work flow with instruction mix table.

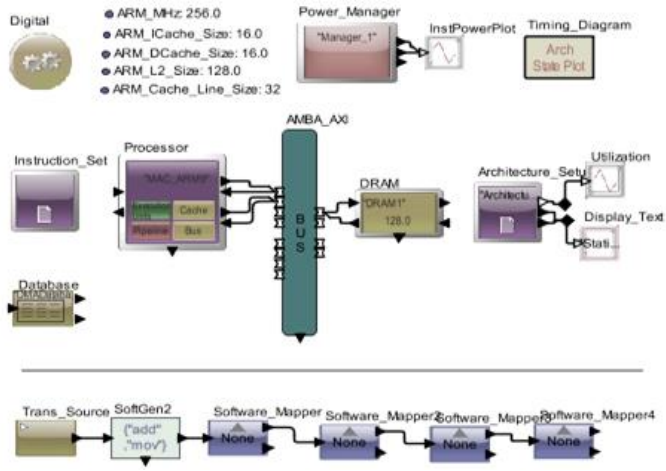

Fig. 5. Hardware accurate modeling,

In this modeling we considered ARM core as hardware component and reconstruction algorithm as software compnent. To generate instrusction mix table tasks of the reconstruction algorithm in MATLAB is first converted to C code then to ARM assembly code and finally Instruction counting and profiling is. Percentage of different types of instruction for respective task is given in the table.

TABLE I. Instruction mix table.

TASK NAME	NO.OF. INST	INT (%)	FP (%)	LOG (%)	I_O (%)	BRCH (%)
Task_1	1146	26	19	24	9	22
Task_2	2033	27	10	11	5	47
Task_3	733	30	8	3	45	14
Task_4	1012	19	2	3	11	65
Task_5	1538	22	23	5	14	36

III. RESULT AND DISCUSSION

Two system latency plots as shown in Fig. 6, first one shows the system latency in which all tasks are considered as equal priority with FCFS scheduling.

System latency increases as simulation time that is because of arrival of the requests in resource queue is increases as simulation time. This is due to request arrival rate is faster than the resource processing speed. In the second case system latency lower that is because of each task having priority and preemptive scheduling algorithm is used. Lowest priority task is preempted by highest priority task that results in initially waiting time of the tasks in the queue less.

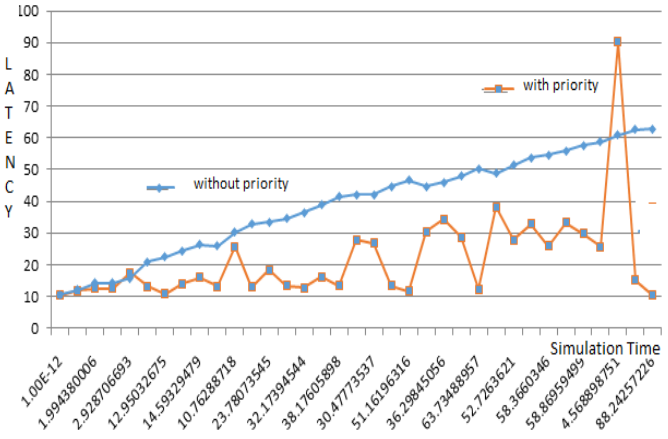

Fig. 6. Latency vs simulation time.

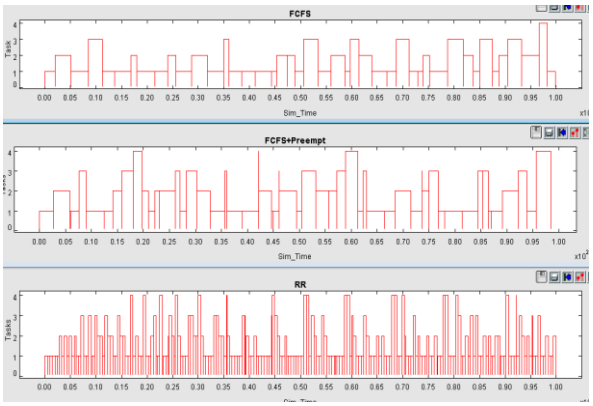

Fig. 7. Task activity timing diagrams.

Using refined queueing model processing of each task can be visualized. Fig. 7 shows the processing activity each task for First Come First Serve(FCFS), Preemptive with FCFS and Round roubin algorithms and system latency of respective scheduling are shown in Fig. 8.

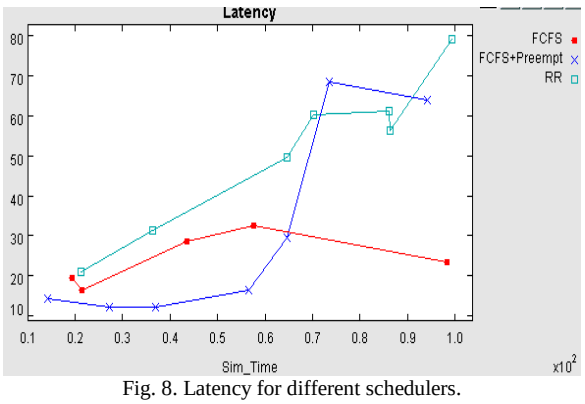

Fig. 8. Latency for different schedulers.

Power modeling shows Instantaneous and average power dissipation since only one resource is used in modeling. Information required to power modeling is number of resource states and power consumption at each state per clock cycle.

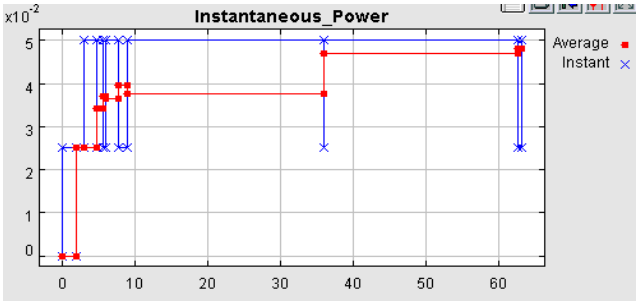

Fig. 9. Instantaneous and average power.

Timing activity of hardware accurate model is shown Fig. 10, here activity of each internal unit of a resource can be visualized and can be identify the idleness of units easily.

Fig. 10. Resources timing activity.

IV. CONCLUSION

Using system level modelling, nonfunctional requirements are analyzed and optimized early in the design stage to achieve efficient system development. In this work system level performance and power modeling concept is discussed and refinements of the model is demonstrated based on available details of the system specification using system engineering tool. Modeling details required to queuing modeling is behavior flow and task processing time, next refined model requires resources speed task scheduling and resources allocation context switching time, power consumption of the resource ate different states is required for power modeling. Design metrics such as latency, throughput, utilization, memory requirements, power consumption and cost can be predicted, analyzed, and optimized using system level modeling.

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